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PIXELPLUS

Preliminary

Datasheet

1/3 inch SD Single Chip CMOS Image Sensor with NTSC/PAL Transmitter

PC1058D

Rev 0.4

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6th Floor, Gyeonggi R&DB Center, 906-5 Iui-dong, Yeongtong-gu,
Suwon-si, Gyeonggi-do, 443-766, Korea
Tel : 82-31-888-5300, FAX : 82-31-888-5398

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    - YCbCr422 / RGB565 / RGB444 / Bayer
  - Analog/Digital Output
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- Image processing on chip : lens shading compensation, gamma correction, defect correction, color correction, NR(2D noise reduction), color interpolation, edge enhancement, brightness, contrast, de-color, auto black level compensation, auto white balance, auto exposure control, back light compensation
- Programmable frame size, window size and position
- Free scaling (scale down)
- Horizontal/Vertical mirroring
- Automatic flicker cancellation
- Smart IR-LED/TDN(moving) filter controller
- 4 overlay functions by using SPI ROM
- I2C master included
- SPI master included
- Software reset
- On-chip phase locked loop (PLL)
- On chip regulator for core
- Crystal input support

General Description

The PC1058D is a 1/3-inch CMOS image sensor with NTSC/PAL Transmitter. It is a single chip with effective pixel array of 968 (width) x 488 (height). The PC1058D can generate analog/digital/composite outputs at maximum frame rate of 60. On-chip sensor functions can be controlled through I2C interface.

Table 1 Key Performance Parameter

Parameter	Typical value
Pixel size	5.0 [um] x 7.40 [um]

Parameter	Typical value
Effective pixel array	968 (H) x 488 (V)
Effective image area	4.840 [mm] x 3.611 [mm]
Optical format	1/3 [inch]
Input clock frequency	27 [MHz]
Output interface	10/8-bit parallel
	CVBS(NTSC/PAL)
Max. frame rate	60fps : ITU-R. BT1302 @ 36[MHz] (for NTSC)
	50fps : ITU-R. BT1302 @ 36[MHz] (for PAL)
	60fields/sec : NTSC @ 36[MHz]
	50fields/sec : PAL @ 36[MHz]
	60fps : YCbCr422/RGB565/RGB444 @ 72[MHz]
	60fps : Bayer @ 36[MHz]
Dark signal	TBD [mV/sec] @ 60 [°C]
Sensitivity	TBD [V/Lux.sec]
Power supply	AVDD : 3.3 [V]
	HVDD : 3.3 [V]
	CVDD : 3.3 [V]
Power consumption	303.6 [mW]@dynamic
	564.2 [uW] @standby
Operating Temp. (fully functional Temp.)	-30~85 [°C] @ ambient
Dynamic range	TBD [dB] @ 60 [°C]
SNR	TBD [dB]

Chip Architecture

The PC1058D has a 972 x 504 total pixel array and includes column/row driver circuits for reading out pixel data progressively. CDS circuit reduces noises generated from various sources, which mainly are resulted from process variations. The fixed errror signal level caused by pixel process variation can be reduced by sampling the defference between the output and the reset level of the pixel. Each of R, G, and B pixel output can be multiplied by different gain factors to balance the color of images under various light conditions. The analog signals are converted into digital data of one line at a time and each line data is streamed out column by column. The Bayer RGB data passes through a sequence of image signal processing to produce various output datas. Image signal processing includes operations such as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. The PC1058D supports various interfaces such as composite, analog, and digital output. The control of internal functions and output signal timings can be enabled by modifying registers directly through a 2-wire serial interface called I2C or by programming the internal/external ROMs which contain device settings.

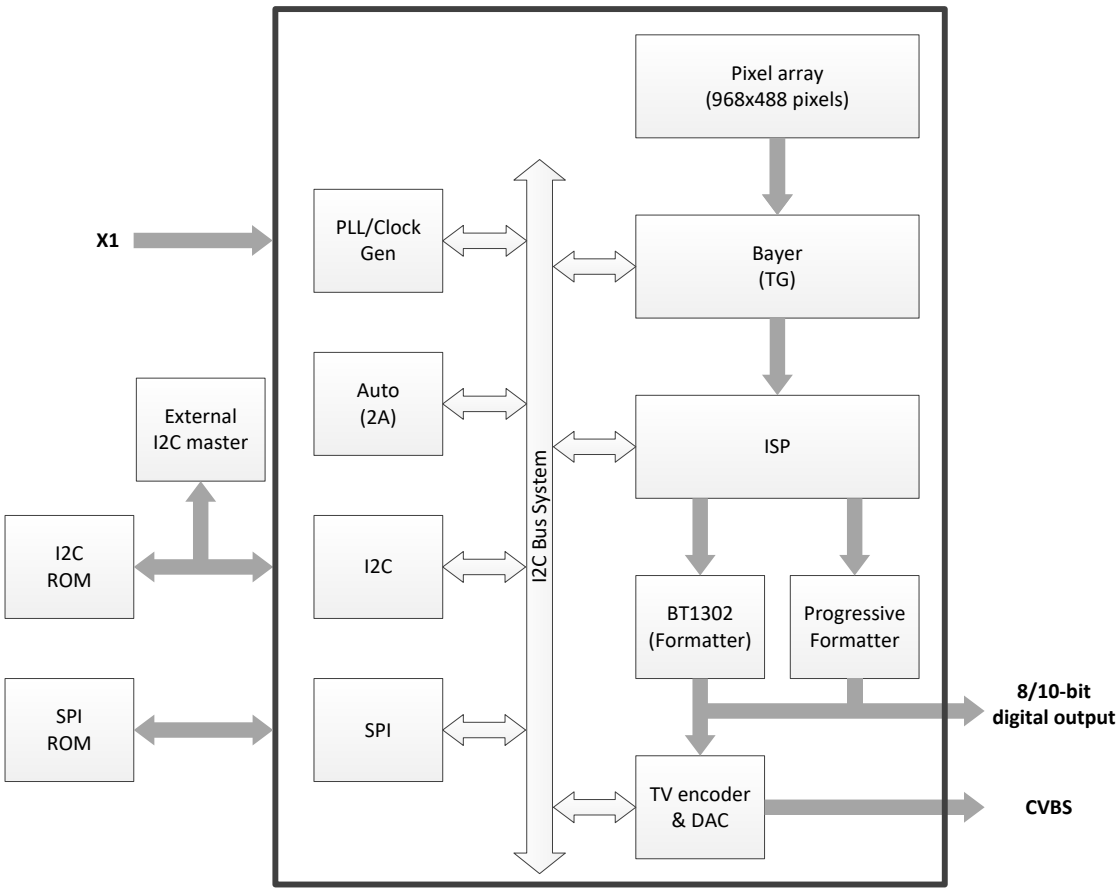


Figure 1 Chip architecture

Frame Structure

The size of a frame is determined by framewidth and frameheight registers. One frame consists of (framewidth + 1) columns and (frameheight + 1) rows, where the size of one frame is allowed to be larger than the total pixel array size. Window determines the output image size, and its default size is 960 x 480 pixels. It is possible to define a specific region of the frame by a determined window. Pixel scanning is performed row by row on entire frame. Frame row counter and frame column counter, which are limited by framewidth and frameheight values respectively, are used to indicate the current coordinate of pixel being scanning. The column counter value increase by every pixel clock (pclk). every time the column counter reaches maximum value, the row counter value increase. Figure 2 shows the default frame structure and the window position of the PC1058D with origin point (0,0) in the top right corner .

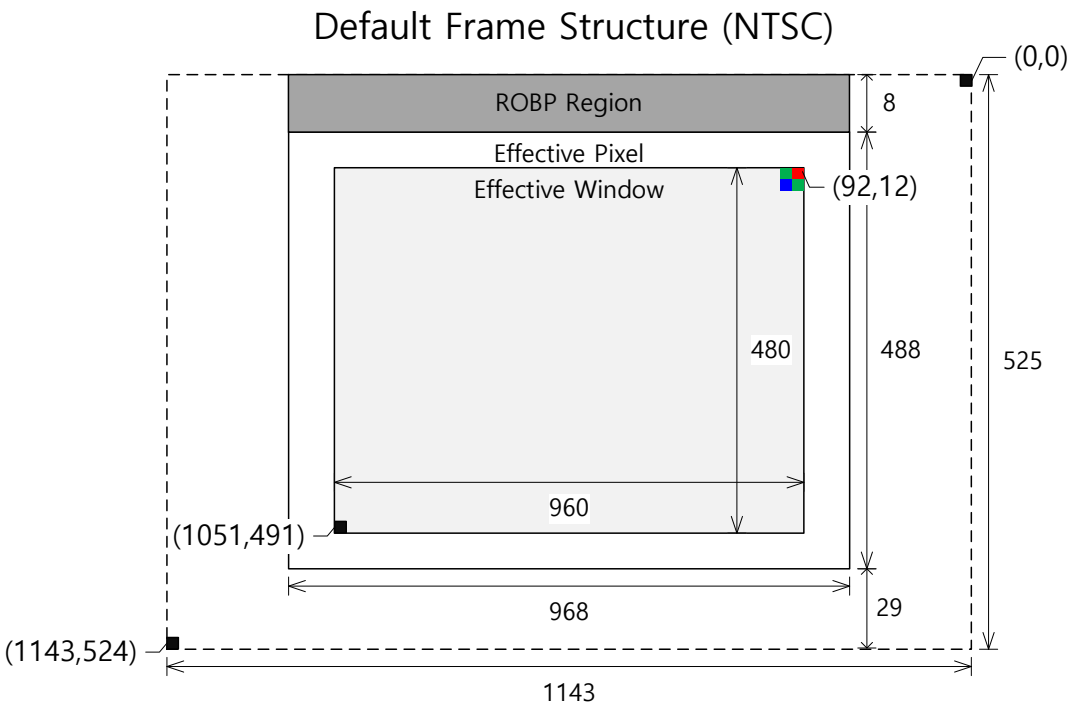


Figure 2 Default frame structure(top view)

Table 2 Register Table - Frame structure

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
framewidth_h	A	06	[3:0]	0xx	RW	aev	Framewidth
framewidth_l	A	07	[7:0]	0xx	RW	aev	
fd_fheight_a_h	A	08	[4:0]	0x02	RW	aev	Frameheight
fd_fheight_a_l	A	09	[7:0]	0xx	RW	aev	
fd_fheight_b_h	A	0A	[4:0]	0x02	RW	aev	
fd_fheight_b_l	A	0B	[7:0]	0xx	RW	aev	
m_tg_frameheight_H	B	E4	[7:0]		RO		Tg frameheight monitoring
m_tg_frameheight_L	B	E5	[7:0]		RO		
m_tg_framewidth_H	B	E6	[7:0]		RO		Tg framewidth monitoring
m_tg_framewidth_L	B	E7	[7:0]		RO		

Data Format

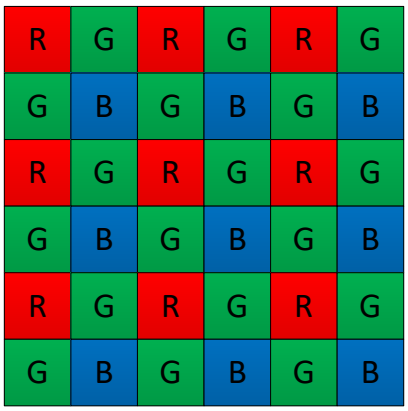


Figure 3 Bayer color filter pattern

Pixel array is covered by Bayer color filters as can be seen in the Figure 3. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PC1058D provides this Bayer pattern RGB data through an 10bit channel. It takes one pclk to pass one pixel RGB data to output bus. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PC1058D adopts a low pass filter to prevent the interference patterns (called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components.

It is possible to extract monochrome luminance data from RGB color components. And the color information is separated from luminance information. Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality. Figure 4 shows 4:2:2 YUV data sequence. PC1058D supports 4:2:2 YUV data format where U and V components are sampled once every two Y components (the format skips one set of U and V components). Therefore, each pixel utilizes one Y component and shares U and V component to represent color and brightness of a pixel.

Figure 4 YUV422 data sequence

Table 3 Register Table - Format control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
format	C	29	[7:0]	0x00	RW	aev	Format control
o8bit	C	9C	[7]	1'b1	RW	aev	8bit output only mode @yuv format

Vsync and Hsync

By manipulating vsyncstartrow_f0, vsyncstoprow_f0, and vsynccolumn register value, start and stop positions of vsync are controlled. sync_drop register allows user to drop vsync or hsync. Figure 5 shows 4 different cases of sync_drop. In addition, sync_hsyncAllLines enables hsync during vsync blank region. Figure 6 shows operation of sync_hsyncAlllines.

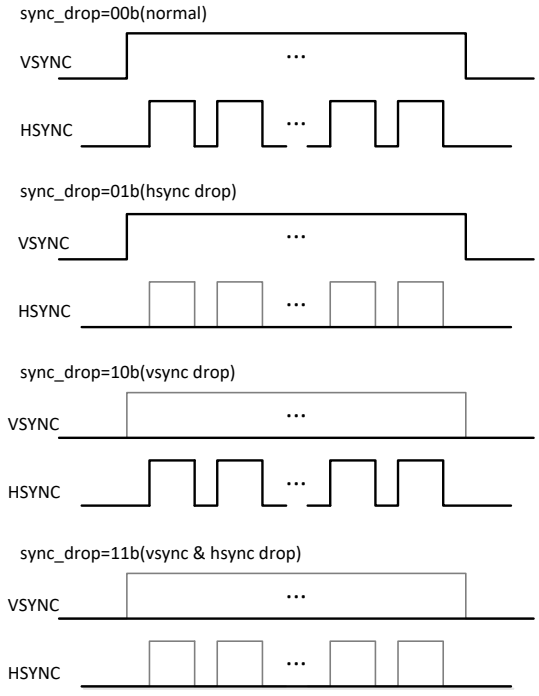


Figure 5 Sync drop

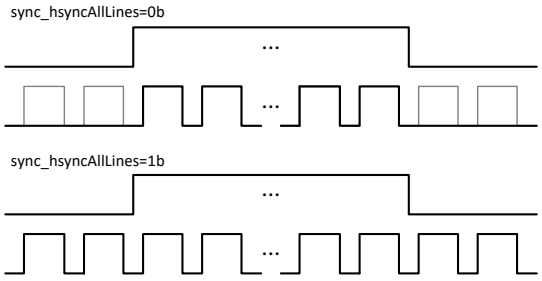


Figure 6 Hsync all lines

sync_vsyncPolarity, sync_hsyncPolarity, sync_pclkPolarity registers invert vsync, hsync, PCLK signal respectively. The inversion functions are shown in Figure 7, Figure 8, Figure 9.

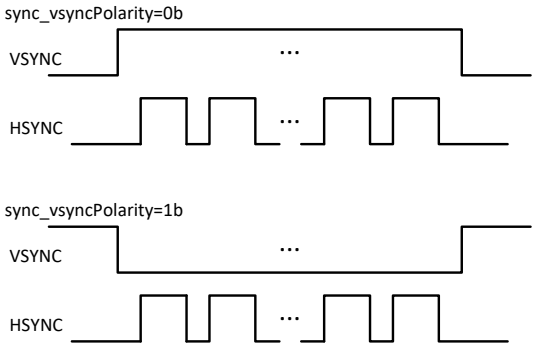


Figure 7 Vsync polarity

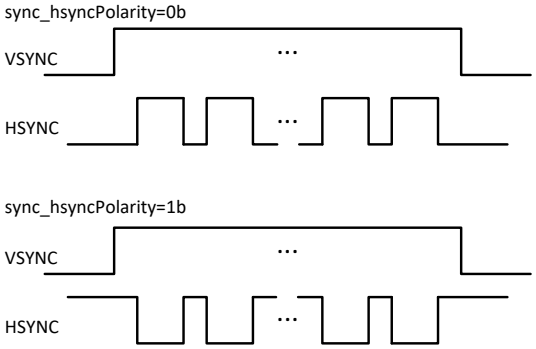


Figure 8 Hsync polarity

Table 4 Register Table - Sync control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
chip_mode	A	04	[1:0]	0xx	RW	aev	chip mode selection 2'b00 : CCIR656 else : N/A
vsyncstartrow_f0_h	A	14	[4:0]	0x00	RW	aev	Vsync generation
vsyncstartrow_f0_l	A	15	[7:0]	0x17	RW	aev	
vsyncstoprow_f0_h	A	16	[4:0]	0x01	RW	aev	
vsyncstoprow_f0_l	A	17	[7:0]	0xx	RW	aev	
vsyncstartrow_f1_h	A	18	[4:0]	0x01	RW	aev	
vsyncstartrow_f1_l	A	19	[7:0]	0xx	RW	aev	
vsyncstoprow_f1_h	A	1A	[4:0]	0x02	RW	aev	
vsyncstoprow_f1_l	A	1B	[7:0]	0xx	RW	aev	
vsynccolumn_h	A	1C	[3:0]	0x00	RW		
vsynccolumn_l	A	1D	[7:0]	0x02	RW		
sync_drop	C	9A	[6:5]	2'b00	RW	aev	2'b00 : disable 2'b01 : hsync drop 2'b10 : vsync drop 2'b11 : hsync and vsync drop

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_vsyncPolarity	C	9B	[6]	1'b0	RW	aev	vsync polarity change
sync_hsyncAllLines	C	9B	[5]	1'b0	RW	aev	hsync output all lines enable(blank and active)
sync_hsyncPolarity	C	9B	[4]	1'b0	RW	aev	hsync polarity change
vsync_pad_en	A	29	[7]	1'b0	RW		vsync pad enable
hsync_pad_en	A	29	[4]	1'b0	RW		hsync pad enable
hsync_drv	A	29	[6:5]	2'b00	RW		hsync pad drivability
pad_drv	A	28	[7:6]	2'b00	RW		vsync, D9~D0 pad drivability

PCLK

PCLK rate is set by dividing pclk, and the division ratio is determined by sync_pclkrate. In addition, PCLK inversion can be enabled via sync_pclkPolarity register as shown in Figure 9.

Table 5 PCLK rate

pclk_rate	PCLK
0d	pclk
1d	pclk x 1/2

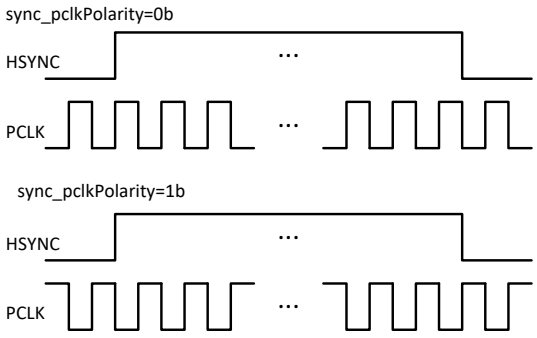


Figure 9 PCLK polarity

Table 6 Register Table - PCLK control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_pclkrate	C	9A	[4:0]	5'b00000	RW	aev	PCLK rate
sync_pclkPolarity	C	9B	[2]	1'b0	RW	aev	PCLK polarity change
pclk_drv	A	28	[5:4]	2'b00	RW		PCLK drivability control
digi_pclk_delay	A	31	[3:0]	4'b0000	RW		PCLK delay control
pclk_pad_en	A	28	[0]	1'b0	RW		PCLK pad enable

Windowing

window sets pixel region displayed to users. The PC1058D outputs pixel data within window where hsync and vsync are high. Registers such as windowx1, windowx2, windowy1, and windowy2 determine the position and size of the window.

upper right corner = (windowx1+1, windowy1)
lower left corner = (windowx2, windowy2-1)

Table 7 Register Table - Window

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
windowx1_h	A	0C	[1:0]	0x00	RW	aev	Window
windowx1_l	A	0D	[7:0]	0x01	RW	aev	
windowy1_h	A	0E	[1:0]	0x00	RW	aev	
windowy1_l	A	0F	[7:0]	0x01	RW	aev	
windowx2_h	A	10	[1:0]	0x03	RW	aev	
windowx2_l	A	11	[7:0]	0xC0	RW	aev	
windowy2_h	A	12	[1:0]	0x01	RW	aev	
windowy2_l	A	13	[7:0]	0xE0	RW	aev	

Scale

Full scaled image pixel location
X point = 32*M
Y point = 32*N
Scaled image sampling point
X Sampling point = scale_x*P
Y Sampling point = scale_y*Q

When scale_x and scale_y are 32d. The scale ratio is 1:1 and the maximum horizontal and vertical scale ratio is 1/8.

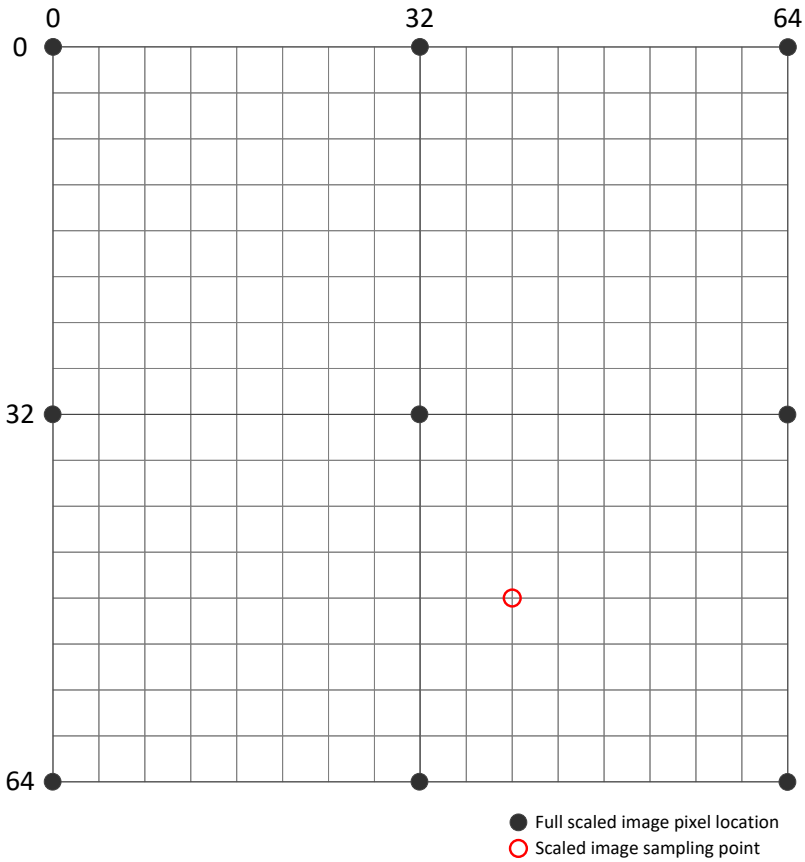


Figure 10 Example of scale down

Table 8 Register Table - Scale

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
scale_x	C	7B	[7:0]	0x20	RW	aev	Horizontal scale factor
scale_y	C	7C	[7:0]	0x20	RW	aev	Vertical scale factor
scale_th_h	C	7D	[2:0]	0x00	RW	aev	Scale buffer TH
scale_th_l	C	7E	[7:0]	0x0A	RW	aev	

ITU-R BT1302

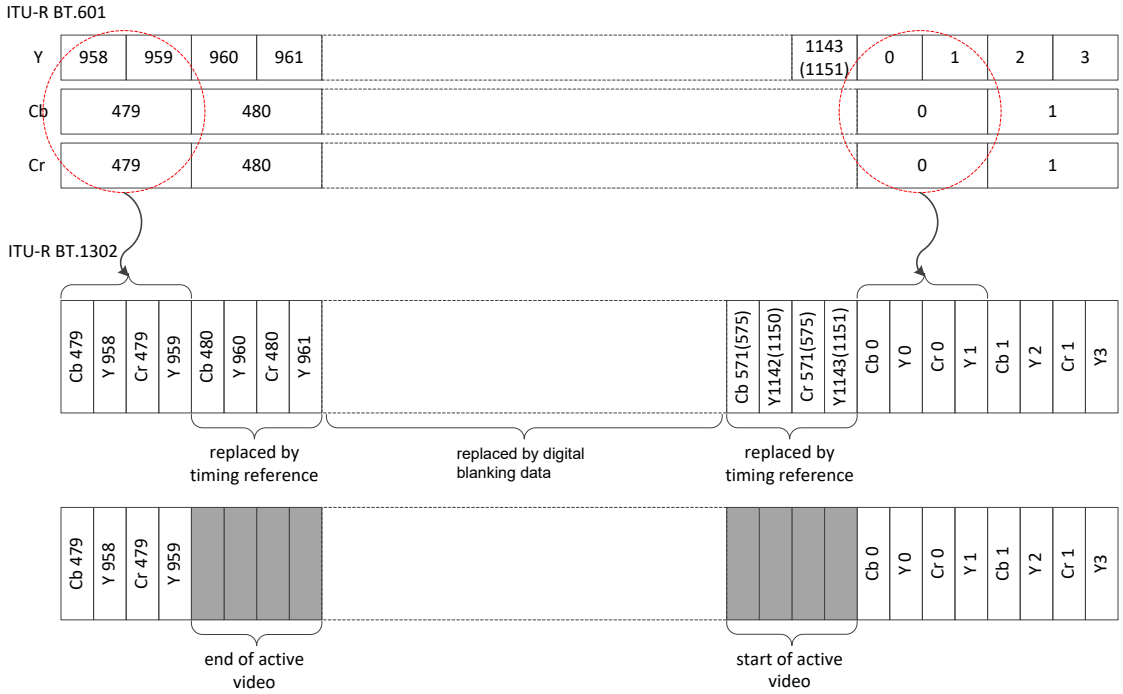


Figure 11 Timing diagram for ITU-R BT1302

Figure 11 shows ITU-R BT601 and ITU-R BT1302 timing diagram. Sampling clocks of ITU-R BT601 and ITU-R BT1302 are 18MHz and 36MHz respectively. ITU-R BT1302 format is generated from ITU-R BT601 format data by serialization and timing reference. Timing reference indicates Start or End of video. It includes field, vsync and hsync information. PC1058D provides two kinds of active video sizes with BT1302 format such as 960x480i and 960x576i (‘i’ stands for interlaced scan). The horizontal size is stretched to 960 pixels. 960x480i size BT1302 supports for 525-line video, and 960x576i size BT1302 for 625-line video. Horizontal timing of 960x480i and 960x576i size BT1302 is shown in Figure 11 and vertical Timing diagram is shown in Figure 12,Figure 13.

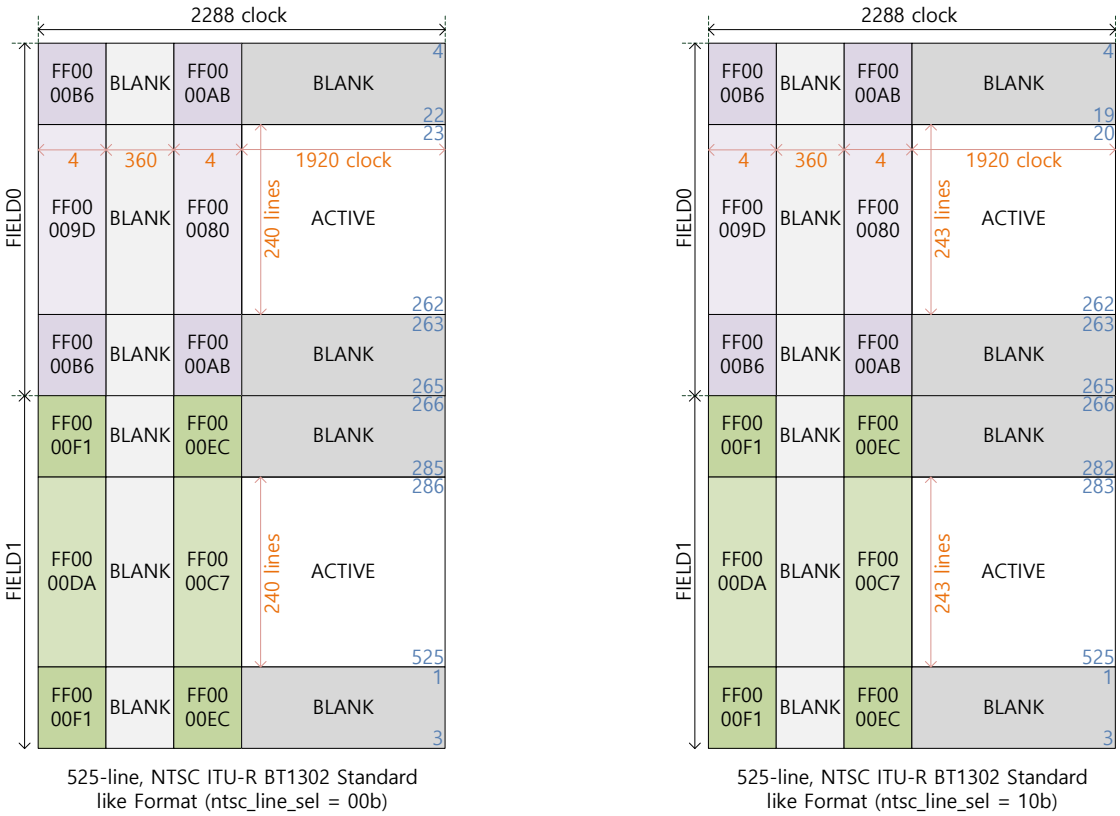


Figure 12 TRS and vertical timing

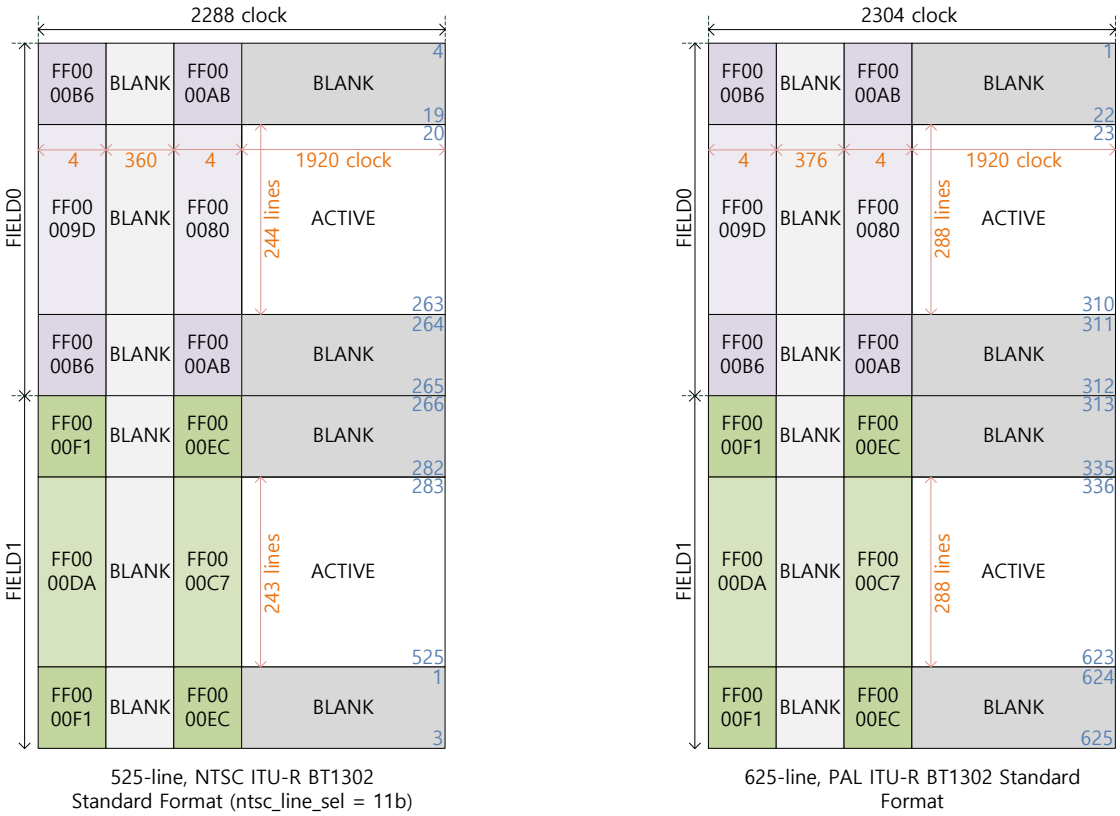


Figure 13 TRS and vertical timing

Table 9 Register Table - ITU-R BT1302

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
xscale_th_h	H	11	[3:0]	0x02	RW		Xscale horizontal scaling TH for encoder
xscale_th_l	H	12	[7:0]	0x80	RW		
x_delay_sel	H	13	[3:0]	0x02	RW		Zoom x delay selection
sync_blankEAV_f0	H	04	[7:0]	0xB6	RW		Blank EAV for field0 of CCIR656 data or blank EAV for frame data
sync_blankSAV_f0	H	05	[7:0]	0xAB	RW		Blank SAV for field0 of CCIR656 data or blank SAV for frame data
sync_activeEAV_f0	H	06	[7:0]	0x9D	RW		Active EAV for field0 of CCIR656 data or active EAV for frame data
sync_activeSAV_f0	H	07	[7:0]	0x80	RW		Active SAV for field0 of CCIR656 data or active SAV for frame data
sync_blankEAV_f1	H	08	[7:0]	0xF1	RW		Blank EAV for field1 of CCIR656 data or blank EAV for frame data
sync_blankSAV_f1	H	09	[7:0]	0xEC	RW		Blank SAV for field1 of CCIR656 data or blank SAV for frame data
sync_activeEAV_f1	H	0A	[7:0]	0xDA	RW		Active EAV for field1 of CCIR656 data or active EAV for frame data

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_activeSAV_f1	H	0B	[7:0]	0xC7	RW		Active SAV for field1 of CCIR656 data or active SAV for frame data
sync_CCIR_FF	H	0C	[7:0]	0xFF	RW		CCIR656 blank data format
sync_CCIR_00	H	0D	[7:0]	0x00	RW		
sync_CCIR_80	H	0E	[7:0]	0x80	RW		
sync_CCIR_10	H	0F	[7:0]	0x10	RW		
d9_pad_en	A	2E	[7]	1'b0	RW		D9 data pad enable
d8_pad_en	A	2E	[6]	1'b0	RW		D8 data pad enable
d7_pad_en	A	2E	[5]	1'b0	RW		D7 data pad enable
d6_pad_en	A	2E	[4]	1'b0	RW		D6 data pad enable
d5_pad_en	A	2E	[3]	1'b0	RW		D5 data pad enable
d4_pad_en	A	2E	[2]	1'b0	RW		D4 data pad enable
d3_pad_en	A	2E	[1]	1'b0	RW		D3 data pad enable
d2_pad_en	A	2E	[0]	1'b0	RW		D2 data pad enable
d1_pad_en	A	29	[3]	1'b0	RW		D1 data pad enable
d0_pad_en	A	29	[2]	1'b0	RW		D0 data pad enable

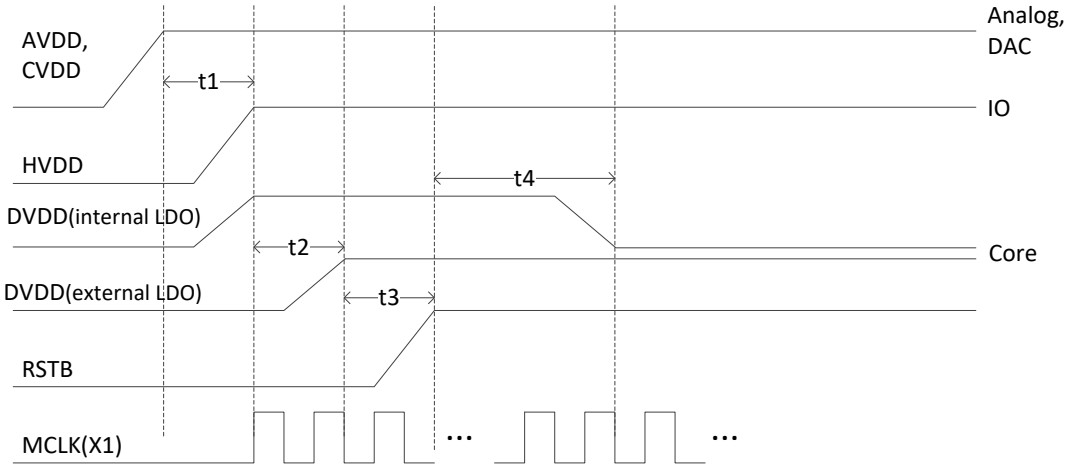
Recommended Power Sequence

Table 10 Recommended power on/down sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From AVDD,CVDD rising to HVDD rising	10	-	-	ms
t2 [a]	From HVDD rising to DVDD(external LDO) rising	10	-	-	ms
t3	Sensor reset time	8	-	-	MCLK
t4 [b]	From RSTB risng to internal LDO power down	10	-	-	ms
t5	From AVDD,CVDD falling to HVDD falling	10	-	-	ms
t6 [c]	From HVDD falling to DVDD(external LDO) falling	10	-	-	ms

[a]You should consider t2 when using external LDO.
[b]You should consider internal LDO power down when using external LDO. You can power down internal LDO though ldo_b_pd, ldo_t_pd registers.
[c]You should consider t6 when using external LDO.

Power-on Sequence(using external LDO)



Power-on Sequence(using internal LDO)

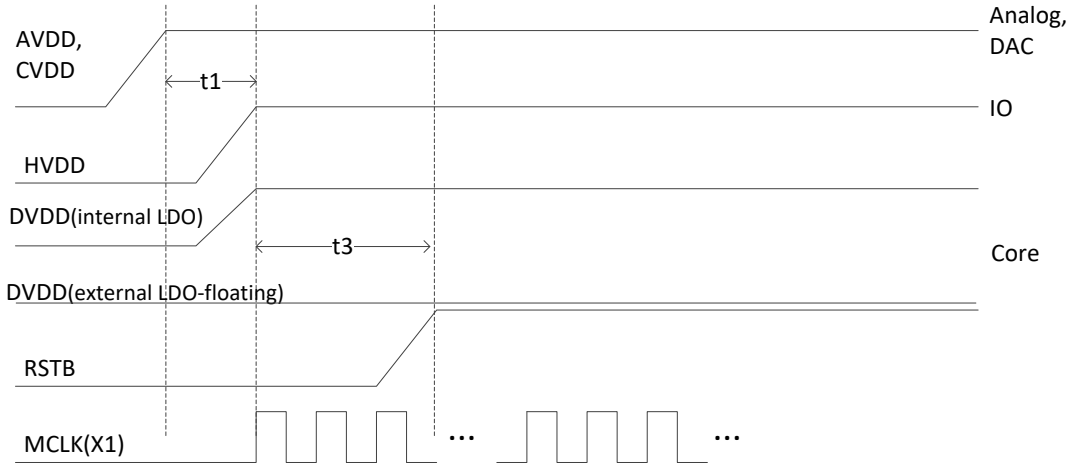


Figure 14 Recommended power on sequence

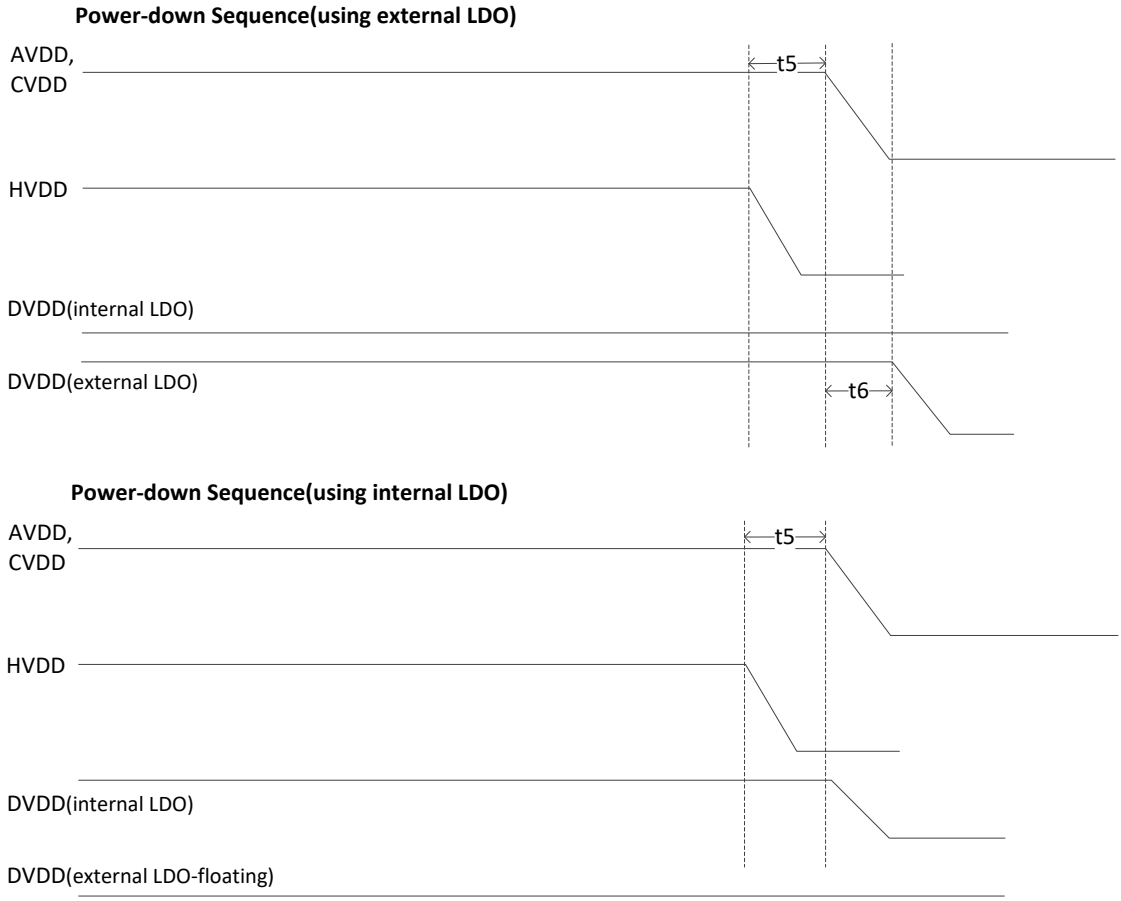


Figure 15 Recommended power down sequence

Clock

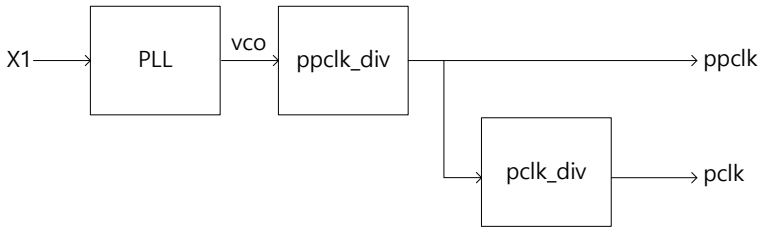


Figure 16 Clock divider

- X1 : PLL input clock
- vco : PLL output clock
- pclk : internal pixel clock
- ppclk : internal double rate pixel clock for progressive parallel output

PLL

Phase-locked loop (PLL) recieves input X1 clock as input reference frequency. X1 frequency is amplified to achieve higher frequency clock. Constraints and basic information on PLL are as follows:

- Frequency of X1(PLL input clock) should be 27MHz.
- Frequency of vco(PLL output clock) should be X1 x pll_ns/pll_ms ≤ 72MHz.
  vco = X1 x pll_ns/pll_ms
- When pll_bypass is set, X1 clock is used instead of vco
- PLL Lock time should be greater than 300us.

Table 11 Register Table - PLL

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pll_ms	A	4D	[7:0]	0x03	RW		PLL division factor
pll_ns	A	4E	[7:0]	0x08	RW		PLL multiplication factor
pll_pd	A	4A	[5]	1'b1	RW		PLL power down 1'b0 : power on 1'b1 : power down
pll_bypass	A	4A	[4]	1'b1	RW		PLL bypass 1'b0 : use pll mode 1'b1 : pll bypass mode

Clock Divider

Table 12 Register Table - Clock divider

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pclk_div	A	25	[5]	1'b1	RW	aev	pclk divider

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b0 : x1/2 1'b1 : x1
ppclk_div	A	25	[2:0]	3'b000	RW	aev	ppclk divider 3'b000 : x1 3'b010 : x1/2 3'b100 : x1/4

PLL and Clock Setting Sequence

- When using PLL, set-up sequence, show Figure 17, is necessary.
- I2C update timing register, i2c_control_1, is changed before setting clock dividers to immediately apply clock divider settings.

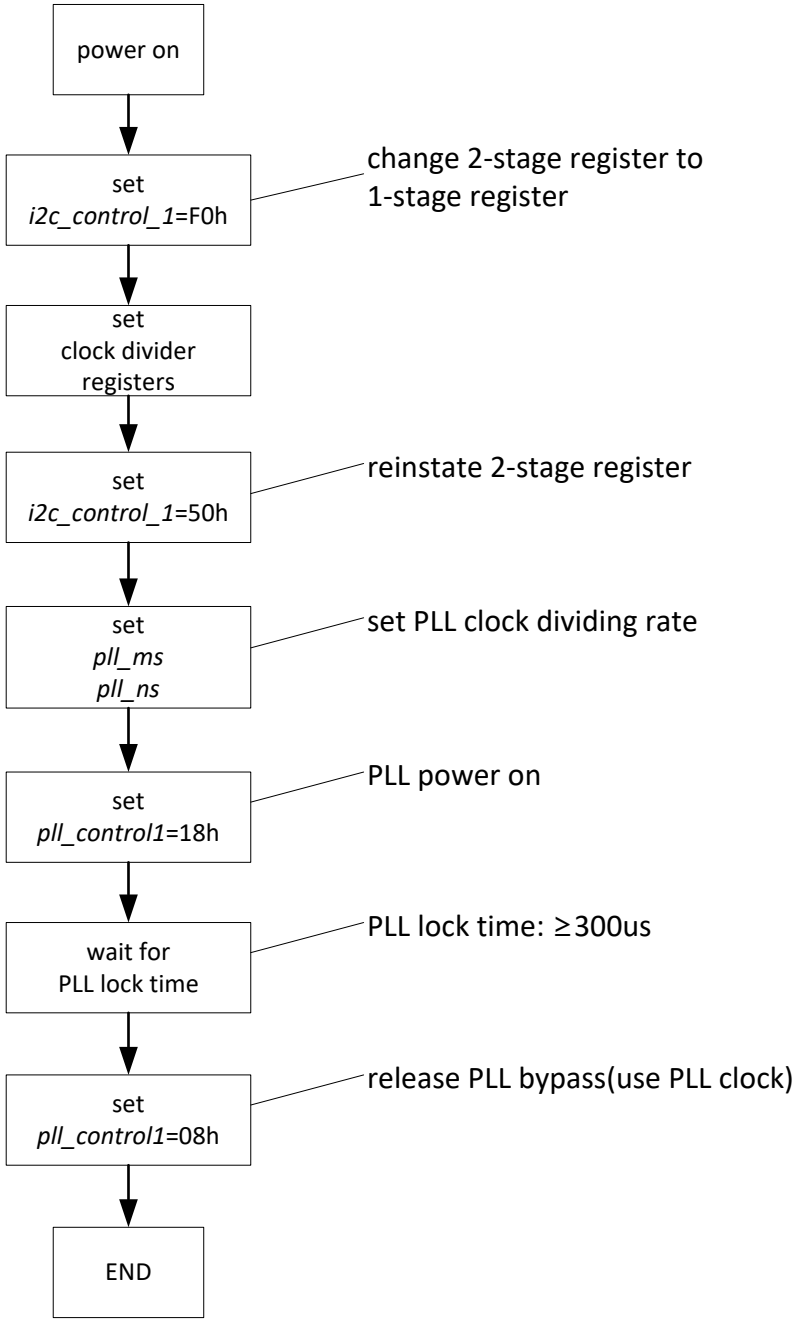


Figure 17 Clock setting sequence

System Reset

The PC1058D has two methods to reset: hard reset and soft reset. Hard reset signal from RSTB PAD must remain low (active low) for at least 8 master clocks to correctly reset the sensor. All registers are set to their default values after reset.

Figure 18 shows device soft reset by setting softreset register through I2C interface. When softreset register is set, async_rstb (asynchronous reset) and sync_rstb signal changes from 1 to 0 and holds for 1 clock of SCL.

Afterward, async_rstb is set back to 1 while sync_rstb holds 0 for another 16 clocks of pclk for stable reset operation. Therefore, PC1058D requires at least 1 clock of SCL and 16 clocks of pclk to perform a soft reset operation.

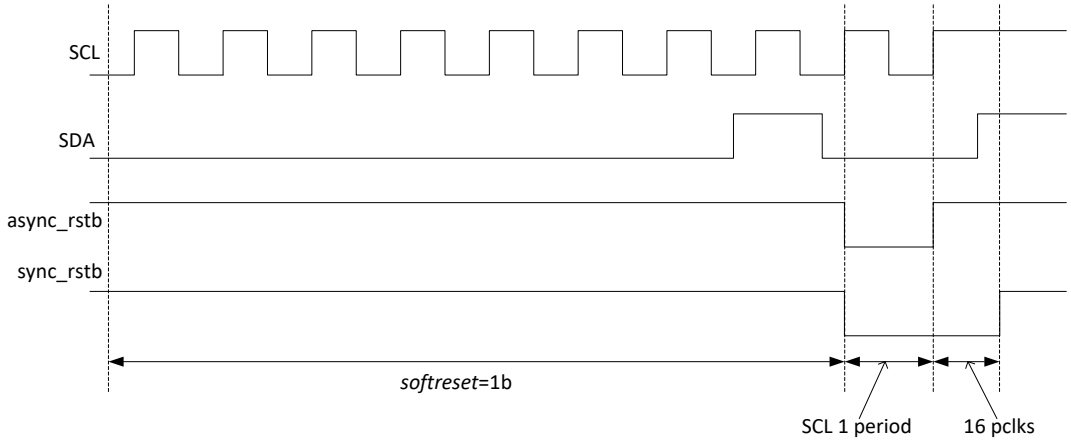


Figure 18 Soft reset

Table 13 Register Table - Soft reset

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
softreset	A	24	[0]	0x00	RW		soft reset

Initialization

Initialization Flow

When power is applied to the chip, an initialization operation is performed. The initialization operation performs different operations depending on the master mode. If master mode is off, initialization is not performed. If master mode is on, start from internal ROM setting. After completing the setting of the internal ROM, the I2C bus must be idle state before entering the next initialization phase.

After internal ROM setting, detection is performed in order of EEPROM and SPI ROM, and if there is no corresponding ROM, jump to the next step. Figure 19 represents the initialization flow.

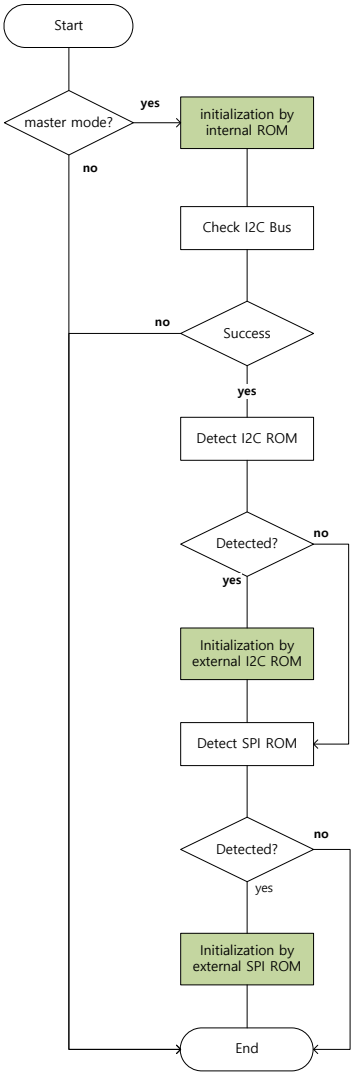


Figure 19 Initialization Flow

PC1058D has a single I2C master and shares the SCL / SDA line with the I2C slave. External I2C master can access PC1058D after Figure 19 process is completed. The initialization time depends on the conditions of master mode and external ROM.

Required Time of Initialization

- Master mode on
  a. In case that external ROM does not exist
     The time to end the internal ROM setting is 7.5 ms.
  b. In case that EEPROM does exist(SCL @ about 300 KHz)
     Cycle time for register write is 200 us
  c. In case that SPI ROM does exist(SCLK @ about 928 KHz)
     Cycle time for register write is 65 us
  d. In master mode, the initialization time is calculated as a + b + c.
- Master mode off

a. Setting time is 0 s.
b. The initialization time is not required when master mode is off.

Wire-strapping

Wire-strapping is a function that can control the setting mode with PAD input. The setting mode is determined by VSYNC, HSYNC, D9 to D0 PAD. Check the PAD input voltage during chip initialization and perform setting according to setting mode. It is shown in setting mode Table 14 according to PAD input voltage.

Table 14 setting mode according to wire-strapping

		vsync	hsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TV Mode	(M)NTSC	-	-	-	-	-	-	-	L	L	L	-	-
	NTSC-J	-	-	-	-	-	-	-	L	L	H	-	-
	(M)PAL	-	-	-	-	-	-	-	L	H	L	-	-
	(Nc)PAL	-	-	-	-	-	-	-	L	H	H	-	-
	(B,D,G,H,I) PAL	-	-	-	-	-	-	-	H	L	L	-	-
	(N)PAL	-	-	-	-	-	-	-	H	L	H	-	-
	NTSC-4.43	-	-	-	-	-	-	-	H	H	L	-	-
Flicker	No Flicker cancel	-	-	-	-	-	L	L	-	-	-	-	-
	Manual-A	-	-	-	-	-	L	H	-	-	-	-	-
	Manual-B	-	-	-	-	-	H	L	-	-	-	-	-
	Auto Flicker cancel	-	-	-	-	-	H	H	-	-	-	-	-
Mirror	NO MIRROR	-	-	-	-	-	-	-	-	-	-	H	L
	MIRROR-V	-	-	-	-	-	-	-	-	-	-	L	L
	MIRROR-H	-	-	-	-	-	-	-	-	-	-	H	H
	MIRROR-VH	-	-	-	-	-	-	-	-	-	-	L	H
BLC (or general[0])	ON	-	-	-	-	H	-	-	-	-	-	-	-
	OFF	-	-	-	-	L	-	-	-	-	-	-	-
Indoor/Outdoor (or general[1])	Indoor mode	-	-	-	H	-	-	-	-	-	-	-	-
	Outdoor mode	-	-	-	L	-	-	-	-	-	-	-	-
OSD Enable	Enable	-	-	H	-	-	-	-	-	-	-	-	-
	Disable	-	-	L	-	-	-	-	-	-	-	-	-
Master Mode	ON	H	-	-	-	-	-	-	-	-	-	-	-
	OFF	L	-	-	-	-	-	-	-	-	-	-	-
General[2]	1'b1	-	H	-	-	-	-	-	-	-	-	-	-
	1'b0	-	L	-	-	-	-	-	-	-	-	-	-

When using general strap, max. gain strap can be used as general [1:0].

Real-time Strap

In general setting mode, the setting can be applied in real time by changing strap_control [2:0]. strap_control [2:0], in turn, matches general [2:0]. If the corresponding bit is set to *0*, settings according to the general setting mode are applied in real time.

Table 15 Register Table - strap_control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
strap_control	A	30	[7:0]	0xFF	RW		general mode real-time setting control [7] : Master mode [6] : General mode [5] : OSD mode [4] : Indoor/Outdoor mode [3] : BLC mode [2] : Flicker mode [1] : Video mode [0] : Mirror mode

Internal ROM

PC1058D reads the data according to the PAD input from the internal ROM and performs setting.

Register settings according to mirror mode are shown in Table 16.

Table 16 Mirror mode

[D1,D0]	2'b00	2'b01	2'b10	2'b11
Register name	V mirror	HV mirror	NO mirror	H mirror
mirror	02	03	00	01

Register settings according to chip mode selection are shown in Table 17.

Table 17 Chip Mode Selection at Master Mode 0

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	(M)NTSC	NTSC-J	(M)PAL	(Nc)PAL	(OTHER)PALs	(N)PAL	NTSC-4.43
chip_mode	00	00	00	01	01	01	00
framewidth_h	04	04	04	05	05	05	04
framewidth_l	77	77	77	67	67	67	77
fd_a_step_h	03	03	03	04	04	04	03
fd_a_step_l	E8	E8	E8	BD	BD	BD	E8
fd_b_step_l	42	42	42	F0	F0	F0	42
fd_period_a_h	01	01	01	00	00	00	01
fd_period_a_m	03	03	03	D8	D8	D8	03
fd_period_a_l	80	80	80	EB	EB	EB	80
fd_period_b_m	3A	3A	3A	01	01	01	3A
fd_period_b_l	F5	F5	F5	00	00	00	F5
fd_period_c_h	06	06	06	05	05	05	06
fd_period_c_m	26	26	26	15	15	15	26
fd_fheight_a_l	0C	0C	0C	07	07	07	0C
fd_fheight_b_l	0C	0C	0C	07	07	07	0C
expfrmH_l	07	07	07	02	02	02	07
midfrmheight_l	07	07	07	02	02	02	07

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	**(M)NTSC**	**NTSC-J**	**(M)PAL**	**(Nc)PAL**	**(OTHER)PALs**	**(N)PAL**	**NTSC-4.43**
maxfrmheight_l	07	07	07	02	02	02	07
vsyncstoprow_f0_l	06	06	06	36	36	36	06
vsyncstartrow_f1_l	1E	1E	1E	50	50	50	1E
vsyncstoprow_f1_l	0D	0D	0D	6F	6F	6F	0D
enc_mode	00	00	03	02	01	01	00
enc_blankL	F0	F0	F0	FC	FC	F0	F0
enc_pedestal	2A	00	2A	00	00	2A	2A
enc_burst	80	82	8C	8A	9C	9A	82
enc_Ygain	82	8D	82	89	89	82	82
enc_Ugain	6F	78	6F	75	75	6F	6F
enc_Vgain	9C	A9	9C	A6	A6	9C	9C
enc_Crange_L	48	62	48	5B	5B	48	48
enc_chroma_max_L	CD	DF	CD	D7	D7	CD	CD
enc_chroma_min_L	6D	35	6D	45	45	6D	6D
enc_scfreq	00	00	03	02	01	01	01

Register settings according to chip mode selection are shown in Table 18.

Table 18 Chip Mode Selection at Master Mode 1

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	**(M)NTSC**	**NTSC-J**	**(M)PAL**	**(Nc)PAL**	**(OTHER)PALs**	**(N)PAL**	**NTSC-4.43**
pll_control1	18	18	18	18	18	18	18
pad_control7	01	01	01	01	01	01	01
chip_mode	00	00	00	01	01	01	00
framewidth_h	04	04	04	05	05	05	04
framewidth_l	77	77	77	67	67	67	77
fd_a_step_h	03	03	03	04	04	04	03
fd_a_step_l	E8	E8	E8	BD	BD	BD	E8
fd_b_step_l	42	42	42	F0	F0	F0	42
fd_period_a_h	01	01	01	00	00	00	01
fd_period_a_m	03	03	03	D8	D8	D8	03
fd_period_a_l	80	80	80	EB	EB	EB	80
fd_period_b_m	3A	3A	3A	01	01	01	3A
fd_period_b_l	F5	F5	F5	00	00	00	F5
fd_period_c_h	06	06	06	05	05	05	06
fd_period_c_m	26	26	26	15	15	15	26
fd_fheight_a_l	0C	0C	0C	07	07	07	0C
fd_fheight_b_l	0C	0C	0C	07	07	07	0C
expfrmH_l	07	07	07	02	02	02	07

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	**(M)NTSC**	**NTSC-J**	**(M)PAL**	**(Nc)PAL**	**(OTHER)PALs**	**(N)PAL**	**NTSC-4.43**
midfrmheight_l	07	07	07	02	02	02	07
maxfrmheight_l	07	07	07	02	02	02	07
vsyncstoprow_f0_l	06	06	06	36	36	36	06
vsyncstartrow_f1_l	1E	1E	1E	50	50	50	1E
vsyncstoprow_f1_l	0D	0D	0D	6F	6F	6F	0D
enc_mode	00	00	03	02	01	01	00
enc_blankL	F0	F0	F0	FC	FC	F0	F0
enc_pedestal	2A	00	2A	00	00	2A	2A
enc_burst	80	82	8C	8A	9C	9A	82
enc_Ygain	82	8D	82	89	89	82	82
enc_Ugain	6F	78	6F	75	75	6F	6F
enc_Vgain	9C	A9	9C	A6	A6	9C	9C
enc_Crange_L	48	62	48	5B	5B	48	48
enc_chroma_max_L	CD	DF	CD	D7	D7	CD	CD
enc_chroma_min_L	6D	35	6D	45	45	6D	6D
enc_scfreq	00	00	03	02	01	01	01
osd_efld_s_h	00	00	00	00	00	00	00
osd_efld_s_l	01	01	01	01	01	01	01
osd_ofld_s_h	01	01	01	01	01	01	01
osd_ofld_s_l	0A	0A	0A	39	39	39	0A
hsync_p_toffset	12	12	13	11	11	08	12
burst_duration	00	00	88	8B	00	00	91
l_blank_start	11	11	11	1C	1E	1D	11
l_blank_stop	03	00	03	0D	0D	00	03
sync_rising	05	05	05	08	0A	09	05
burst_toffset	89	89	0C	8D	99	99	89
encdat_rising	05	05	05	09	0A	09	05
setup_w	09	00	09	00	00	09	09
pll_control1	08	08	08	08	08	08	08
pg_yt	7F	7F	7F	7F	7F	7F	7F
pg_y1	73	73	73	8C	8C	8C	73
pg_y2	02	02	02	02	02	02	02
pg_y3	08	08	08	08	08	08	08
pg_y4	0F	0F	0F	11	11	11	0F
pg_y5	19	19	19	1C	1C	1C	19
pg_y6	25	25	25	2A	2A	2A	25
pg_y7	28	28	28	2D	2D	2D	28
pg_y8	38	38	38	40	40	40	38

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	**(M)NTSC**	**NTSC-J**	**(M)PAL**	**(Nc)PAL**	**(OTHER)PALs**	**(N)PAL**	**NTSC-4.43**
pg_y9	4E	4E	4E	59	59	59	4E
pg_y10	52	52	52	5D	5D	5D	52
pg_a	BF	BF	BF	BF	BF	BF	BF
pg_b	81	81	81	76	76	76	81
pg_c	BF	BF	BF	BF	BF	BF	BF
pg_d	0B	0B	0B	0B	0B	0B	0B
pg_e	0C	0C	0C	0A	0A	0A	0C
pg_f	15	15	15	15	15	15	15
pg_line1	21	21	21	21	21	21	21
pg_line2	23	23	23	23	23	23	23
pg_line3	24	24	24	26	26	26	24
pg_line4	46	46	46	47	47	47	46
pg_line5	48	48	48	4A	4A	4A	48
pg_line6	42	42	42	42	42	42	42
pg_line7	4B	4B	4B	4E	4E	4E	4B
pg_line8	71	71	71	74	74	74	71
pg_line9	63	63	63	63	63	63	63
pg_line10	74	74	74	7A	7A	7A	74
hs_th2_m	1F	1F	1F	09	09	09	1F
midexp_h	47	47	47	42	42	42	47
midexp_m	E0	E0	E0	40	40	40	E0
maxexp_h	8F	8F	8F	84	84	84	8F
maxexp_m	C0	C0	C0	80	80	80	C0
min_yt1	98	98	98	98	98	98	98
ygm1_y1	0C	0C	0C	04	04	04	0C
ygm1_y2	20	20	20	11	11	11	20
ygm1_y3	2F	2F	2F	20	20	20	2F
ygm1_y4	3A	3A	3A	2D	2D	2D	3A
ygm1_y5	4B	4B	4B	42	42	42	4B
ygm1_y6	58	58	58	52	52	52	58
ygm1_y7	6D	6D	6D	6A	6A	6A	6D
ygm1_y8	7F	7F	7F	7D	7D	7D	7F
ygm1_y9	9C	9C	9C	9B	9B	9B	9C
ygm1_y11	CA	CA	CA	C9	C9	C9	CA
ygm1_y12	DD	DD	DD	DD	DD	DD	DD
ygm1_y13	EF	EF	EF	EF	EF	EF	EF
ygm2_y1	11	11	11	09	09	09	11
ygm2_y2	1B	1B	1B	10	10	10	1B

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	**(M)NTSC**	**NTSC-J**	**(M)PAL**	**(Nc)PAL**	**(OTHER)PALs**	**(N)PAL**	**NTSC-4.43**
ygm2_y3	23	23	23	16	16	16	23
ygm2_y4	2A	2A	2A	1C	1C	1C	2A
ygm2_y5	37	37	37	27	27	27	37
ygm2_y6	42	42	42	30	30	30	42
ygm2_y7	56	56	56	43	43	43	56
ygm2_y8	68	68	68	54	54	54	68
ygm2_y9	87	87	87	75	75	75	87
ygm2_y10	A3	A3	A3	93	93	93	A3
ygm2_y11	BC	BC	BC	B0	B0	B0	BC
ygm2_y12	D4	D4	D4	CB	CB	CB	D4
ygm2_y13	EA	EA	EA	E6	E6	E6	EA
cgm2_y1	07	07	07	0B	0B	0B	07
cgm2_y2	0D	0D	0D	13	13	13	0D
cgm2_y3	13	13	13	1A	1A	1A	13
cgm2_y4	18	18	18	20	20	20	18
cgm2_y5	22	22	22	2B	2B	2B	22
cgm2_y6	2C	2C	2C	36	36	36	2C
cgm2_y7	3E	3E	3E	49	49	49	3E
cgm2_y8	4F	4F	4F	5A	5A	5A	4F
cgm2_y9	6F	6F	6F	7B	7B	7B	6F
cgm2_y10	8E	8E	8E	98	98	98	8E
cgm2_y11	AC	AC	AC	B4	B4	B4	AC
cgm2_y12	C8	C8	C8	CE	CE	CE	C8
cgm2_y13	E4	E4	E4	E7	E7	E7	E4
ccr_m21	86	86	86	8A	8A	8A	86
ccr_m22	37	37	37	36	36	36	37
ccr_m23	91	91	91	8C	8C	8C	91
ccr_m31	83	83	83	01	01	01	83
ccr_m32	9C	9C	9C	A6	A6	A6	9C
ccr_m33	3F	3F	3F	45	45	45	3F
cs11_a	38	38	38	36	36	36	38
cs12_a	1C	1C	1C	18	18	18	1C
cs21_a	82	82	82	02	02	02	82
cs22_a	2C	2C	2C	28	28	28	2C
cs11_c	27	27	27	26	26	26	27
cs22_c	24	24	24	23	23	23	24
dark_ec_mth1	20	20	20	04	04	04	20
dark_ec_mth2	30	30	30	04	04	04	30

[D4,D3,D2]	3'b000	3'b001	3'b010	3'b011	3'b100	3'b101	3'b110
Register name	**(M)NTSC**	**NTSC-J**	**(M)PAL**	**(Nc)PAL**	**(OTHER)PALs**	**(N)PAL**	**NTSC-4.43**
ybrightness_ref1	0	0	0	04	04	04	0
ybrightness_ref2	0	0	0	08	08	08	0
dark_ec_pmax2	20	20	20	7F	7F	7F	20
dark_ec_mmax2	10	10	10	7F	7F	7F	10
dark_dc1	8	8	8	00	00	00	8
y_cont_slope2_ref0	42	42	42	40	40	40	42
y_cont_slope2_ref1	42	42	42	40	40	40	42
y_cont_slope2_ref2	44	44	44	40	40	40	44

Register settings according to flicker mode are shown in Table 19.

Table 19 Flicker mode

[D6,D5]	2'b00	2'b01	2'b10	2'b11
Register name	**Normal(off)**	**manual A**	**manual B**	**auto fd**
flicker_control1	00	08	04	40

Register settings according to BLC mode are shown in Table 20.

Table 20 BLC mode at Master Mode 1

[D7]	"0b"	"1b"
Register name	**BLC off**	**BLC on**
ae_weight1	08	08
ae_weight2	08	08
ae_weight3	08	08
ae_weight4	08	08
ae_weightc	08	38

Register settings according to indoor/outdoor mode are shown in Table 21.

Table 21 Indoor/outdoor mode at Master Mode 1

[D8]	"0b"	"1b"
Register name	**Outdoor**	**Indoor**
awb_rgain_min1	64	00
awb_rgain_min2	64	00
awb_rgain_max1	90	FF
awb_rgain_max2	90	FF
awb_bgain_min1	54	00
awb_bgain_min2	54	00
awb_bgain_max1	68	FF
awb_bgain_max2	68	FF

Register settings according to master mode are shown in Table 22

Table 22 Different register settings according to Master Mode

[vsync]	"0b"	"1b"		[vsync]	"0b"	"1b"	
Register name	**master off**	**NTSC**	**PAL**	**Register name**	**master off**	**NTSC**	**PAL**
osd_efld_s_h	00	00	00	maxexp_h	03	8F	84
osd_efld_s_l	01	01	01	maxexp_m	00	C0	80
osd_ofld_s_h	01	01	01	min_yt1	78	98	98
osd_ofld_s_l	0A	0A	39	ygm1_y1	03	0C	04
hsync_p_toffset	00	12	11	ygm1_y2	0C	20	11
burst_duration	00	00	00	ygm1_y3	19	2F	20
l_blank_start	00	11	1E	ygm1_y4	26	3A	2D
l_blank_stop	00	03	0D	ygm1_y5	3F	4B	42
sync_rising	01	05	0A	ygm1_y6	52	58	52
burst_toffset	00	89	99	ygm1_y7	6E	6D	6A
encdat_rising	01	05	0A	ygm1_y8	82	7F	7D
setup_w	07	09	00	ygm1_y9	A1	9C	9B
pll_control1	38	08	08	ygm1_y11	CE	CA	C9
pg_yt	7F	7F	7F	ygm1_y12	E0	DD	DD
pg_y1	73	73	8C	ygm1_y13	F0	EF	EF
pg_y2	02	02	02	ygm2_y1	0B	11	09
pg_y3	08	08	08	ygm2_y2	17	1B	10
pg_y4	0F	0F	11	ygm2_y3	22	23	16
pg_y5	19	19	1C	ygm2_y4	2E	2A	1C
pg_y6	25	25	2A	ygm2_y5	40	37	27
pg_y7	28	28	2D	ygm2_y6	50	42	30
pg_y8	38	38	40	ygm2_y7	6E	56	43
pg_y9	4E	4E	59	ygm2_y8	88	68	54
pg_y10	52	52	5D	ygm2_y9	AE	87	75
pg_a	BF	BF	BF	ygm2_y10	CA	A3	93
pg_b	81	81	76	ygm2_y11	DC	BC	B0
pg_c	BF	BF	BF	ygm2_y12	EC	D4	CB
pg_d	0B	0B	0B	ygm2_y13	F6	EA	E6
pg_e	0C	0C	0A	cgm2_y1	0B	07	0B
pg_f	15	15	15	cgm2_y2	17	0D	13
pg_line1	21	21	21	cgm2_y3	22	13	1A
pg_line2	23	23	23	cgm2_y4	2E	18	20
pg_line3	24	24	26	cgm2_y5	40	22	2B
pg_line4	46	46	47	cgm2_y6	50	2C	36
pg_line5	48	48	4A	cgm2_y7	6E	3E	49
pg_line6	42	42	42	cgm2_y8	88	4F	5A
pg_line7	4B	4B	4E	cgm2_y9	AE	6F	7B

[vsync]	"0b"	"1b"		[vsync]	"0b"	"1b"	
Register name	**master off**	**NTSC**	**PAL**	**Register name**	**master off**	**NTSC**	**PAL**
pg_line8	71	71	74	cgm2_y10	CA	8E	98
pg_line9	63	63	63	cgm2_y11	DC	AC	B4
pg_line10	74	74	7A	cgm2_y12	EC	C8	CE
hs_th2_m	1F	1F	09	cgm2_y13	F6	E4	E7
midexp_h	81	47	42	ccr_m21	8A	86	8A
midexp_m	80	E0	40	ccr_m22	32	37	36
maxexp_h	03	8F	84	ccr_m23	88	91	8C
maxexp_m	00	C0	80	ccr_m31	83	83	01
min_yt1	78	98	98	ccr_m32	9C	9C	A6
ygm1_y1	03	0C	04	ccr_m33	3F	3F	45
ygm1_y2	0C	20	11	cs11_a	28	38	36
ygm1_y3	19	2F	20	cs12_a	00	1C	18
ygm1_y4	26	3A	2D	cs21_a	00	82	02
ygm1_y5	3F	4B	42	cs22_a	28	2C	28
ygm1_y6	52	58	52	cs11_c	20	27	26
ygm1_y7	6E	6D	6A	cs22_c	20	24	23
ygm1_y8	82	7F	7D	dark_ec_mth1	40	20	04
ygm1_y9	A1	9C	9B	dark_ec_mth2	80	30	04
ygm1_y11	CE	CA	C9	ybrightness_ref1	00	00	04
ygm1_y12	E0	DD	DD	ybrightness_ref2	00	00	08
ygm1_y13	F0	EF	EF	dark_ec_pmax2	7F	20	7F
ygm2_y1	0B	11	09	dark_ec_mmax2	7F	10	7F
ygm2_y2	17	1B	10	dark_dc1	00	08	00
ygm2_y3	22	23	16	y_cont_slope2_ref0	40	42	40
ygm2_y4	2E	2A	1C	y_cont_slope2_ref1	40	42	40
ygm2_y5	40	37	27	y_cont_slope2_ref2	40	44	40

External ROM

External ROM Structure

Address[29:0] = Segment Descriptor

Address	Contents
0	ABh(constant)
1	CDh(constant)
2	reserved
3	reserved
4	reserved
5	reserved
6~7	Common Segment Start
8~9	Common Segment Stop
10~11	TV_mode Segment Start
12~13	TV_mode Segment Stop
14~15	Mirror Segment Start
16~17	Mirror Segment Stop
18~19	Flicker Segment Start
20~21	Flicker Segment Stop
22~23	General Segment Start
24~25	General Segment Stop
26~27	LED Segment Start
28~29	LED Segment Stop

Address	Contents
...	...
Common Start Common Stop	Common Segment
TV_mode Start	NTSC
TV_mode Stop	PAL
Mirror Start	Mirror = 00
	Mirror = 01
	Mirror = 10
Mirror Stop	Mirror = 11
Flicker Start	Flicker = 00
	Flicker = 01
	Flicker = 10
Flicker Stop	Flicker = 11
General Start	General = 000
	...
	...
	...
General Stop	General = 111
LED Start	LED on
LED Stop	LED off

Figure 20 External ROM structure

Figure 20 shows external ROM structure. The user can use the external ROM to apply settings differently depending on the strap input or the external environment. The external ROM consists of the following segments.

Common segment : Regardless of the strap, it is set in the external ROM initialization process.
TV mode segment : Depending on the tv_mode strap, the settings are applied differently.
Mirror segment : Depending on the mirror strap, the settings are applied differently.
Flicker segment : Depending on the flicker strap, the settings are applied differently.
PLL segment : Depending on the pll strap, the setting are applied differently.
General segment : Depending on the general strap(General[2] strap, max. gain strap), the settings are applied differently
LED segment : Depending on the LED on/off, the settings are applied differently.

EEPROM

EEPROM can be used as External ROM. The SCL and SDA lines are pulled up to HVDD by a off-chip resistor of $2[k\Omega]$.

I2C Baud Rate

I2C baud rate is fixed to 385 Kbps.

SPI ROM

The SPI ROM can be used as the external ROM, and all segments can be used in the SPI ROM.

SPI Baud Rate

Table 23 Register Table - SPI baud rate

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
spi_baud_rate	F	69	[3:0]	0x0D	RW		SPI baud rate

spi_baud_rate determines the SPI communication speed. According to register setting, it is divided at the same rate as Table 24.

Table 24 SPI baud rate - SCLK frequency

spi_baud_rate	SCK freq.(MHz)
0d	sif_clk/1
1d	sif_clk/2
2d	sif_clk/3
3d	sif_clk/4
4d	sif_clk/5
5d	sif_clk/6
6d	sif_clk/7
7d	sif_clk/8
8d	sif_clk/10
9d	sif_clk/12
10d	sif_clk/14
11d	sif_clk/16
12d	sif_clk/24
13d	sif_clk/32
14d	sif_clk/48
15d	sif_clk/80

SPI ROM Command

The command value registers for communicating with the SPI ROM are shown in Table 25. Since the command may be different for each manufacturer of SPI ROM, the related register can be changed by command.

Table 25 Register Table - SPI ROM command

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
spi_cmd_we	F	A3	[7:0]	0x06	RW		SPI command
spi_cmd_se	F	A4	[7:0]	0xD8	RW		
spi_cmd_pp	F	A5	[7:0]	0x02	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
spi_cmd_rs	F	A6	[7:0]	0x05	RW		
spi_pad_en	A	2B	[7]	1'b1	RW		
spi_pad_drv	A	2B	[5:4]	2'b00	RW		

SPI PAD Control

To communicate with the SPI ROM, the SPI PAD must be enabled.
Table 26 is a list of registers related to the SPI PAD control.

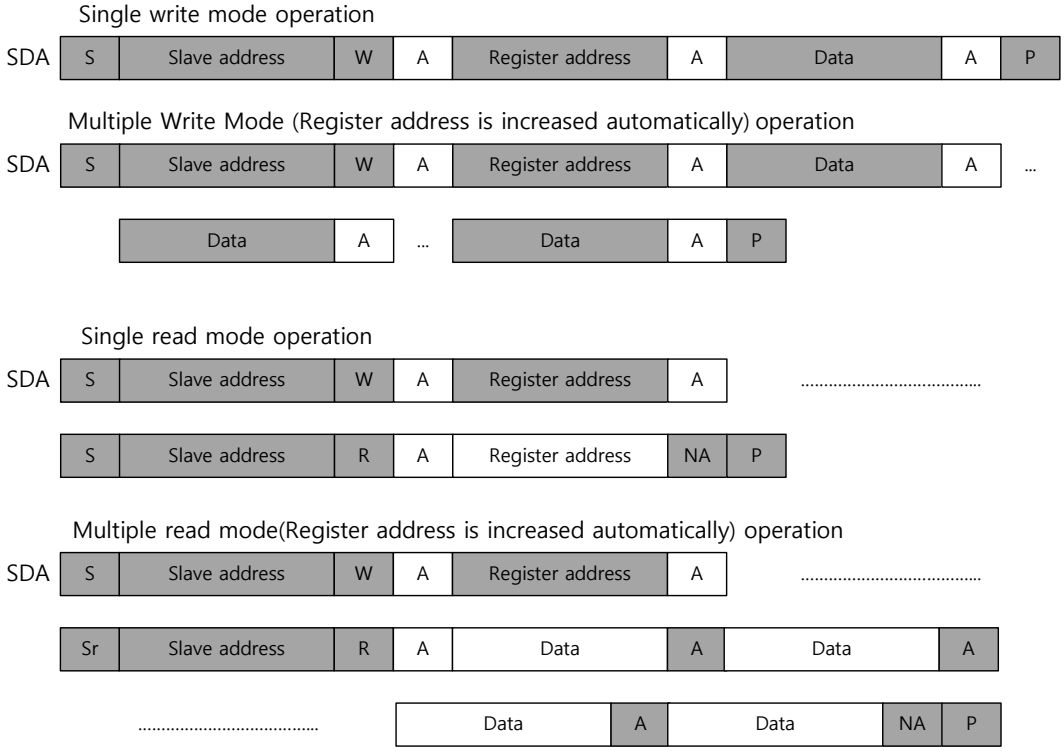
Table 26 Register Table - SPI PAD control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
spi_pad_en	A	2B	[7]	1'b1	RW		SPI pad enable
spi_pad_drv	A	2B	[5:4]	2'b00	RW		SPI pad drivability

External Communication Specification

I2C Communication

I2C communication is a serial interface which utilizes SCL/SDA lines to transfer 8-bit data per transaction. The SCL and SDA lines are pulled up to HVDD by a off-chip resistor of $2[k\Omega]$. PC1058D includes only I2C slave function and requires external master to access the internal registers. Each transaction requires 8-bit data and 1-bit acknowledge bit. There are four types of operations supported in PC1058D's I2C operation: single write, multiple write, single read, multiple read.
In single write operation, after the start state, 7-bit slave address and write bit are transmitted from master device to PC1058D. If correct slave address is detected, PC1058D reply with acknowledge bit as confirmation of valid address. Then master device transmits register address and waits for acknowledge bit from PC1058D. Lastly, 8-bit data is sent to PC1058D and waits for acknowledge bit again. Once acknowledge bit is recieved, master device announces the stop state to terminate I2C communication.
Multiple write operation works exactly the same until stop state procedure. Instead of announcing the stop state, master device transmits more data. If PC1058D detects multiple write operation, any data stream following the first 8-bit is stored in subsequent register addresses of the first register address.
Read operation consists of two sub-procedure: address write and data read. The procedure is performed exactly same as register address write procedure from single write operation. Afterward, master device announces repeated start and transmit slave address with read bit. When PC1058D detects read operation, PC1058D sends acknowledge bit to master device, then reads register corresponding to register address. PC1058D transmits read data to master device and waits for master device to respond. If master device responds with no acknowledge bit followed by stop state, read operation is terminated. On the other hand, if master device responds with acknowledge, PC1058D reads the subsequent register and transmits again. As long as master device replies with acknowledge bit after each data transaction, PC1058D will continuously read the subsequent register and transmit until no acknolwedge bit followed by stop state is presented. If only one 8-bit data is read, the procedure is single read operation. whereas, reading more than 8-bit data is multiple read operation. Figure 21 shows read/ write operation of I2C communication.



Slave address is fixed

write address	read address
66h	67h

R/W : Read/Write selection, High = read / Low = write
A : Acknowledge bit, NA : No Acknowledge, DATA : 8-bit data. P : Stop condition
S : Start condition, Sr : Repeated start(start without preceding stop)

Figure 21 I2C functional description

Register Update Timing

Registers has three different types of update timing: "aev" and "autov" update, regular update. Registers with "aev" and "autov" update type update new values from I2C write operation at the last line of the frame. Whereas, registers with regular update type apply new values immediately after I2C write operation. However, By changing updatecontrol register value, register updates for "aev" and "autov" type can either be disabled or be updated immediately.

Table 27 I2C update timing control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
updatecontrol	A	23	[7:4]	4'b0101	RW		Control i2c register update update_autov <= updatecontrol[3] or (autov_update and updatecontrol[2]) update_aev <= updatecontrol[1] or

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							(aev_update and updatecontrol[0])

SPI

SPI communication is a serial interface consisting of 4 lines of SCK, CSB, MISO and MOSI. PC1058D communicates with the external SPI ROM via the internal SPI Master.

SPI Communication

Figure 22 shows SPI communication read, write enable, sector erase, page program, and read status regsiter operations.

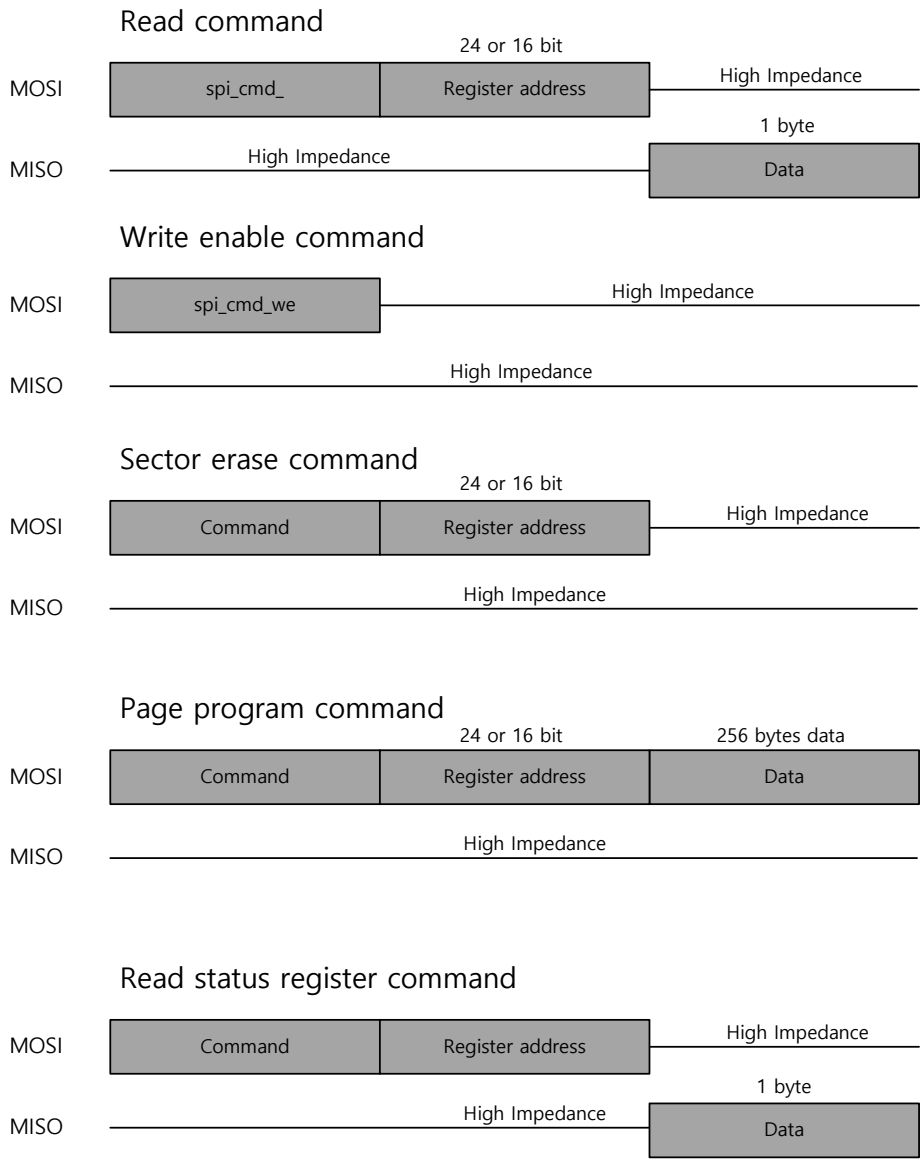


Figure 22 SPI functional description

Flicker Cancelation

PC1058D includes flicker cancelation feature. Generally, operating frequency of light source is either 60 Hz or 50 Hz. Therefore, PC1058D's flicker cancelation feature is pre-configured states with 60 Hz light source frequency as state A and 50 Hz light source frequency as state B.
Three different flicker cancelation mode is available in PC1058D: auto mode, manual A mode, and manual B mode.

- Auto mode(fd_en = 1'b1, manual_A = 1'b0, manual_B = 1'b0)
  When flicker in image is detected, current state is toggled. In other word, current state is switched to the other state.

- manual_A mode(fd_en = 1'b0, manual_A = 1'b1, manual_B = 1'b0)
  Manual A mode puts flicker cancelation state in state A regardless of flicker. Factory setting of PC1058D is configured for 60 Hz light source.

- manual_B mode(fd_en = 1'b0, manual_A = 1'b0, manual_B = 1'b1)
  Manual B mode puts flicker cancelation state in state B regardless of flicker. Factory setting of PC1058D is configured for 50 Hz light source.

Table 28 shows registers relevant to flicker cancelation.

Table 28 Register Table - Flicker cancelation

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
fd_en	A	4F	[6]	1'b0	RW		auto flicker detection enable
manual_A	A	4F	[3]	1'b0	RW		Manual flicker cancellation state control
manual_B	A	4F	[2]	1'b0	RW		

LED Control

LED control functions include IRLED control with Cds, LED blinking.

The IRLED control function uses infrared light by operating the external IRLED in low light conditions where there is not enough visible light. real_led_data means the amount of light absorbed by Cds. IRLED control function has auto mode and manual mode.

- ledctl en = 1'b1 (auto mode)
  When real_led_data is less than led_lvth1, 1'b1 (LED on) signal is output. When real_led_data is greater than led_lvth2, it outputs 1'b0 (LED off) signal. The led_frame is a value that delays the IRLED on / off transition. The unit of led_frame is frame. (refet to Figure 23)

- ledctl en = 1'b0 (manual mode)
  The ledctl manual controls the IRLED control output. When ledctl manual is set to 1'b1, it outputs LED on signal, If ledctl manual is set to 1'b0, it outputs LED off signal.

Bwled en is a function that changes the screen to black and white in LED on operation.

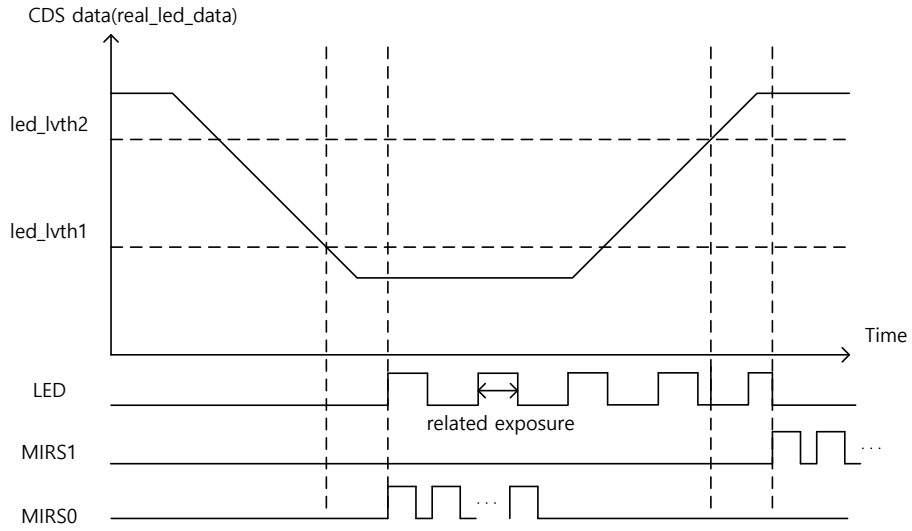


Figure 23 LED control with CdS

Table 29 Register Table - LED control with CdS

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
led_lvth1	A	90	[7:0]	0x00	RW		LED control level threshold 1
led_lvth2	A	91	[7:0]	0x00	RW		LED control level threshold 2
led_frame	A	92	[7:0]	0x80	RW		LED control wait period in frame unit
ledctrl_en	A	2A	[7]	1'b0	RW		LED_CTRL PAD control 1'b0: disable 1'b1: enable
ledctl en	A	8E	[7]	1'b0	RW		LED control enable 1'b0: disable 1'b1: enable
ledctl manual	A	8E	[6]	1'b0	RW		LED manual control 1'b0: disable 1'b1: enable @ ledctl en = 1'b0
ledctl polarity	A	8E	[5]	1'b0	RW		LED output polarity inversion 1'b0: disable 1'b1: enable
bwled en	A	8E	[4]	1'b0	RW		LED black and white enable
led_dsel	B	15	[1:0]	2'b01	RW		LED data selection
inv_led	B	16	[2]	1'b0	RW		LED data inverting enable 1'b0 : disable 1'b1 : enable
real_led_data	B	D7	[7:0]		RO		Current CdS data
mirsctrl_en	A	2C	[7]	1'b0	RW		mirs control enable 1'b0 : diable 1'b1 : enable
mirs en	A	8E	[3]	1'b0	RW		moving IR/AR glass switch (mirs) control enable 1'b0 : disable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b1 : enable
mirsctrl_pad_drv	A	2C	[6:5]	2'b00	RW		mirs pad drivability control
mirs manual	A	8E	[2:1]	2'b00	RW		mirs output value @ mirs control disable
mirs polarity	A	8E	[0]	1'b0	RW		mirs output polarity change enable 1'b0 : disable 1'b1 : enable
mirs_pw	A	93	[7:0]	0x64	RW		mirs pulse width control
mirs_pp	A	95	[7:0]	0xC8	RW		mirs pulse period control
mirs_cnt	A	96	[7:0]	0x01	RW		the number of mirs pulses control

Exposure Control

Integration Time

PC1058D employs rolling shutter [1] for capturing image. Reset operation initializes ROBP and active pixel region in sequence row by row. Readout process reads pixel data stored in photodetector at the identical order and speed as reset operation. The difference in time between reset and readout operation is known as integration time (refer to Figure 24). Integration time controls photodetector's level of exposure to light. Integration time can be adjusted in line unit level (line inttime) and column unit level (column inttime). Under the assumption of fixed frame structure, the maximum line inttime is "frame height - 5" and column inttime is "frame width - 1". Upper 16 bits of inttime register represent number of lines for line inttime and lower 8 bits of inttime register represent number of column inttime, where number of column changes in framewidth/256 increment. Trade-off relationship can be set between integration time and frame rate by enabling frame variable mode. If frmvar_en=1'b1 and integration time is larger than the frame height, the system accommodates the integration time by changing the maximum frame height internally. Due to this process, overall frame structure increases which results in decrease in frame rate.

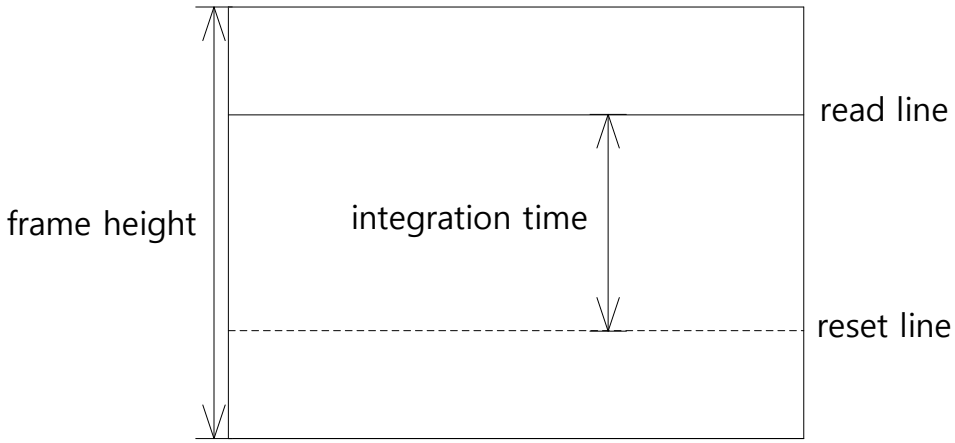


Figure 24 Fundamental concept of integration time

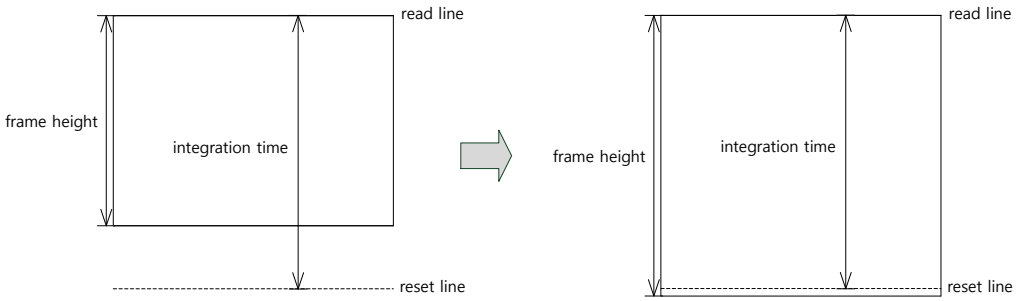


Figure 25 Integration time with frame variable mode enabled

[1] Image capture method in which each frame is scanned row by row instead of capturing entire frame at once

Table 30 shows registers relevant to integration time.

Table 30 Register Table - Integration time

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
inttime_h	B	BC	[7:0]	0x01	RW	aev	Integration time (line)
inttime_m	B	BD	[7:0]	0x40	RW	aev	
inttime_l	B	BE	[7:0]	0x00	RW	aev	Integration time (column)
frmvar_en	B	15	[6]	1'b0	RW		Frame rate variable mode 1'b0: disable 1'b1: enable
m_inttime_tgout_H	B	E9	[7:0]		RO		Tg integration time monitoring
m_inttime_tgout_M	B	EA	[7:0]		RO		
m_inttime_tgout_L	B	EB	[7:0]		RO		

Global Gain

Global gain affects analog gain level of comparators, which determines Bayer data values.

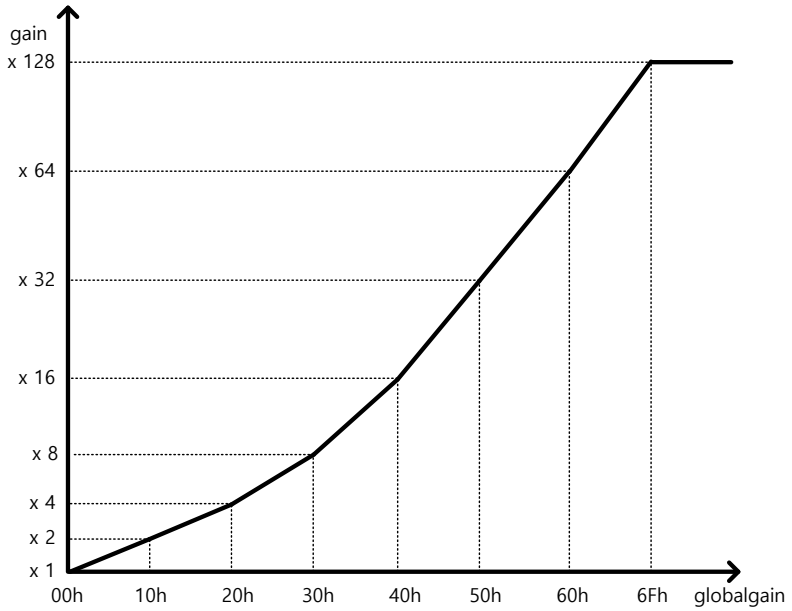


Figure 26 Globalgain's gain

Table 31 shows registers relevant to global gain.

Table 31 Register Table - Global Gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
globalgain	B	BF	[7:0]	0x00	RW	aev	Analog gain
globalgain_max	B	F4	[7:0]	0x5F	RW		Max. analog gain

Digital Gain

Analog signal is converted to digital value through ADC operation, and the digital value can be amplified by digital gain. digitalgain register's upper 2 bits are positive integer and lower 6 bits are fraction.

Table 32 shows registers relevant to digital gain

Table 32 Register Table - Digital gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
digitalgain	B	C0	[7:0]	0x40	RW	aev	Digital gain

Recommended Exposure Setting Procedure

Due to exposure controls being split across several registers, all exposure related registers, such as inttime, global gain, and digital gain, needs to be updated simultaneously to ensure reliable exposure update. It is recommended to disable "aev" type registers updates before updating exposure registers. Disabling "aev" type updates can be achieved by setting i2c_control = 0. Once exposure register updates are disabled, user can set the exposure value safely. New exposure value is applied to next frame after reverting i2c_control register to default value. Figure 27 shows sequence of recommended exposure setting

Note If recommended exposure setting procedure is not followed for setting exposure registers, then it may not update all the new exposure values in one frame.

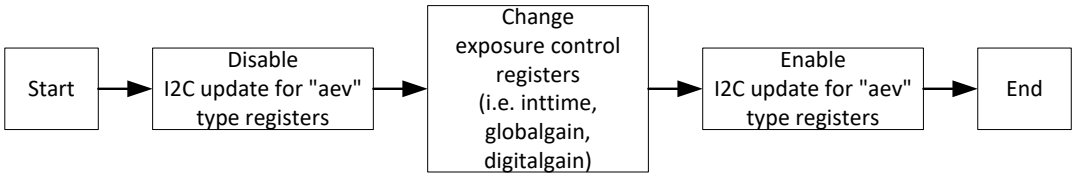


Figure 27 Recommended exposure setting sequence

Black Level Compensation (BLC) Control

Digital black level compensation (BLC) evaluates reference black level based on row optical black pixel (ROBP) and subtracts black level from active pixel value.

Front Black Fitting and Evaluation

Front black is used as an offset value to black level in BLC calculation.

- if dblc_mode = 1'b0, 8-bit 1's complement number representation, which ranges from -127 to 127, is used.
- if dblc_mode = 1'b1, 8-bit positive real number is used, front black value can range from 0 to 255.
- if "front_black fitting" = 1'b0, front_black_ref0 becomes front black value.
- if "front_black fitting" = 1'b1, front_black_ref0~7 are used as reference points for linear fitting respect to global gain.

Figure 28 shows an example of front black fitting.

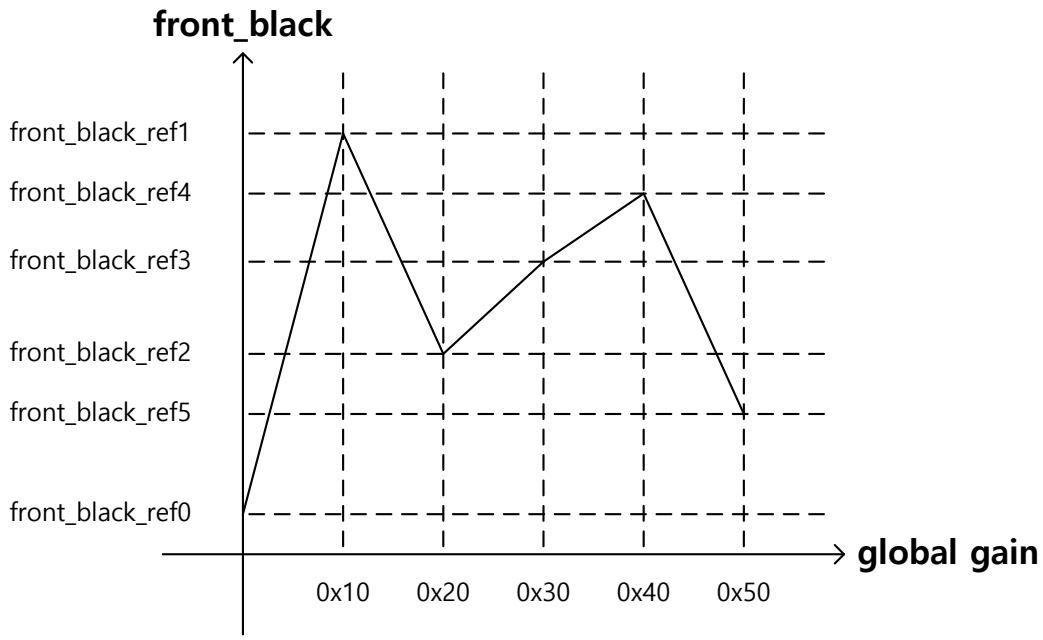


Figure 28 Example of front black fitting

Table 33 shows registers relevant to front black fitting and evaluation.

Table 33 Register Table - Front black

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
fb gg	E	05	[3]	1'b0	RW	autov	Global gain selection in front black fitting

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b0 : high sensitivity conversion gain 1'b1 : normal gain
front_black fitting	E	06	[4]	1'b0	RW	autov	Front black fitting control 1'b0: disable 1'b1: enable
front_black	B	A8	[7:0]	0x00	RW	aev	Front black value
front_black_ref0	B	A0	[7:0]	0x00	RW		Front black fitting points @ front_black_fit_en=1'b1
front_black_ref1	B	A1	[7:0]	0x00	RW		
front_black_ref2	B	A2	[7:0]	0x00	RW		
front_black_ref3	B	A3	[7:0]	0x00	RW		
front_black_ref4	B	A4	[7:0]	0x00	RW		
front_black_ref5	B	A5	[7:0]	0x00	RW		
front_black_max	B	A7	[7:0]	0x7F	RW		Front black maximum value
front_black_min	B	A6	[7:0]	0xFF	RW		Frtont black minumum value
dblc_mode	B	1E	[3]	1'b0	RW		Number representation control 1'b0: 1's compliment number 1'b1: natural number

ISP(Image Signal Processing)

Test Pattern (TP) Control

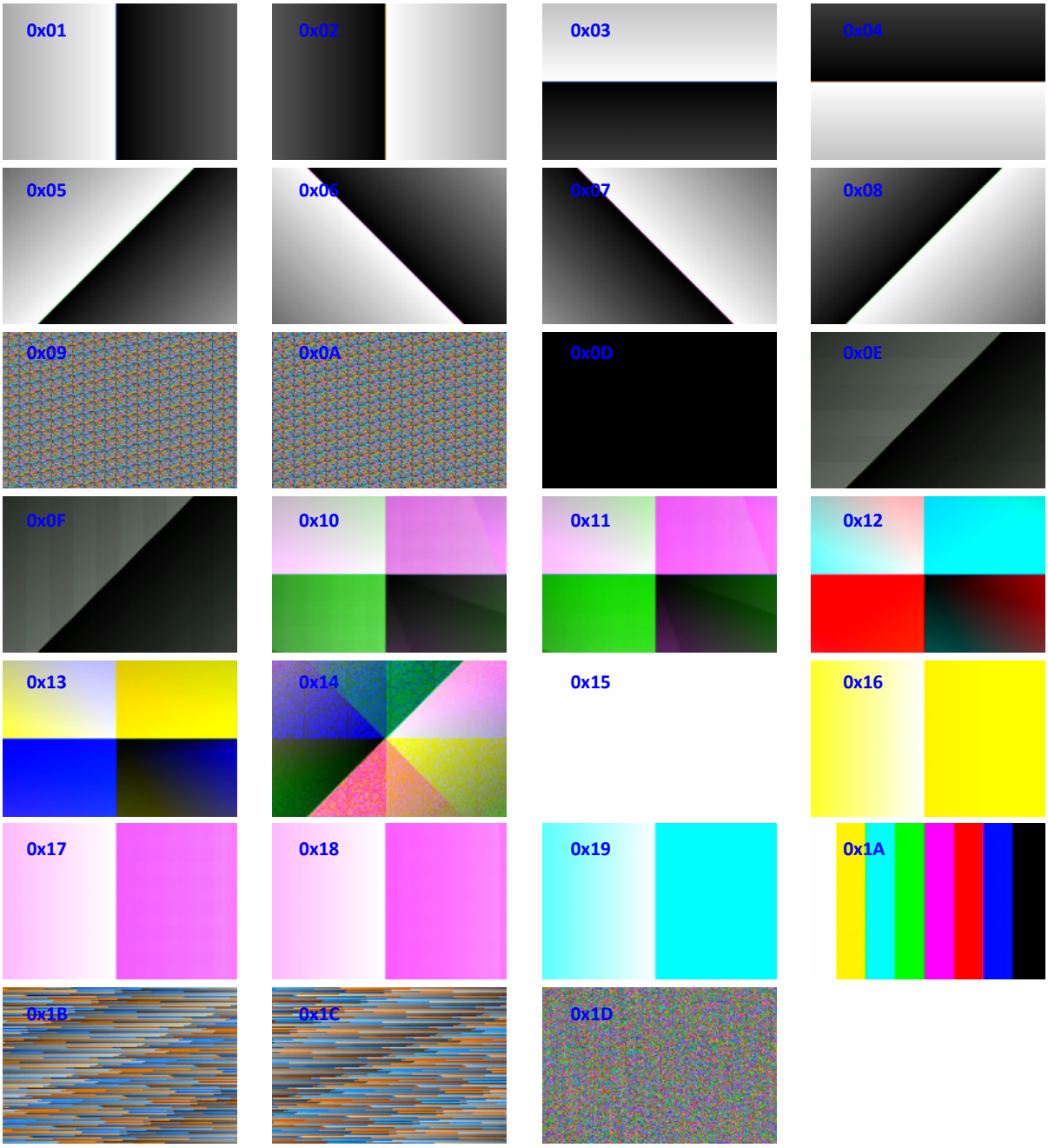
TP control generates test images from ISP block. Test images type can be selected by setting tp_control_0 registers. In case of test image types from 0x15 to 0x1A values for tp_control_0, front_black_ref1/2/3/4/5 registers are used as color values and the following rule shows how the color value is determined:

- R : {front_black_ref1, front_black_ref5[7:6]}
- G1 : {front_black_ref2, front_black_ref5[5:4]}
- G2 : {front_black_ref3, front_black_ref5[3:2]}
- B : {front_black_ref4, front_black_ref5[1:0]}

Table 34 shows registers relevant to Test Pattern Control

Table 34 Register Table - ISP test pattern

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
tp_control_0	C	0C	[7:0]	0x00	RW		Test image selection
front_black_ref1	B	A1	[7:0]	0x00	RW		R[9:2] value for test image
front_black_ref2	B	A2	[7:0]	0x00	RW		Gr[9:2] value for test image
front_black_ref3	B	A3	[7:0]	0x00	RW		Gb[9:2] value for test image
front_black_ref4	B	A4	[7:0]	0x00	RW		B[9:2] value for test image
front_black_ref5	B	A5	[7:0]	0x00	RW		{R[1:0], G1[1:0], G2[1:0], B[1:0]} value for test image



[front_black_ref1, front_black_ref2, front_black_ref3, front_black_ref4, front_black_ref5 = 0xFF]

Figure 29 ISP test pattern

Lens Shading Compensation (LSC)

Pixel sensor residing in edge of the lens receives less light, whereas ample light exposure is obtained in center pixels. LSC feature compensates this uneven distribution of light exposure. By setting lens_en = 1'b1, LSC feature is enabled. LSC function control components are LSC center, LSC scale, and LSC gain.

- LSC center
  By setting lens_x and lens_y, LSC center is adjusted as shown in Figure 30. This parameter is adjusted if the center of the image is not lined up with the center of the lens.

- LSC scale
  By setting lens_scale, scale rate of lens gain from the LSC center is adjusted. lens_scale value is directly proportional to lens gain value.

- LSC gain
  Lens gain of R, G1, G2, B channel can be separately adjusted through lens_gainr, lens_gaing1, lens_gaing2, and lens_gainb registers respectively. Setting high value to the registers result in high lens gain.

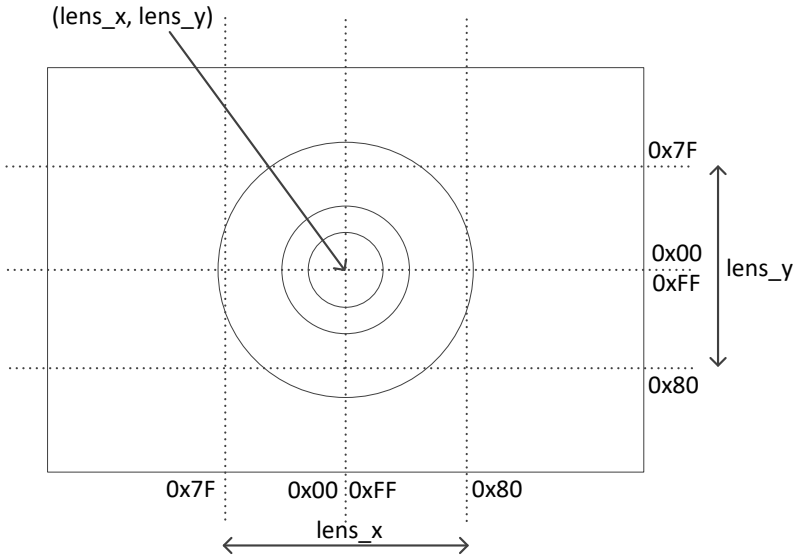


Figure 30 LSC center control

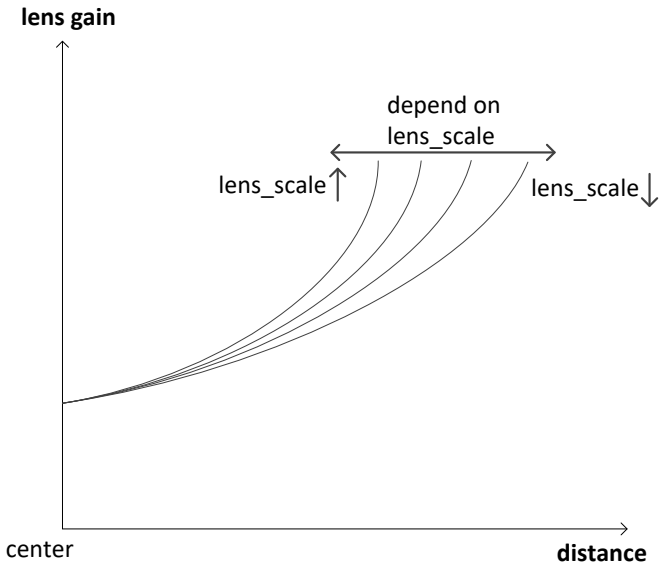


Figure 31 LSC gain fitting with LSC center and LSC scale

Table 35 shows registers relevant to LSC functions.

Table 35 Register Table - LSC

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
lens_en	C	04	[7]	1'b1	RW	aev	Lens shading compensation enable 1'b0 : disable 1'b1 : enable
lens_red_e	C	0D	[7:0]	0x51	RW		Lens shading scale control
lens_red_w	C	0E	[7:0]	0x51	RW		
lens_red_n	C	0F	[7:0]	0x51	RW		
lens_red_s	C	10	[7:0]	0x51	RW		
lens_g1_e	C	11	[7:0]	0x51	RW		
lens_g1_w	C	12	[7:0]	0x51	RW		
lens_g1_n	C	13	[7:0]	0x51	RW		
lens_g1_s	C	14	[7:0]	0x51	RW		
lens_g2_e	C	15	[7:0]	0x51	RW		
lens_g2_w	C	16	[7:0]	0x51	RW		
lens_g2_n	C	17	[7:0]	0x51	RW		
lens_g2_s	C	18	[7:0]	0x51	RW		
lens_blu_e	C	19	[7:0]	0x51	RW		
lens_blu_w	C	1A	[7:0]	0x51	RW		
lens_blu_n	C	1B	[7:0]	0x51	RW		
lens_blu_s	C	1C	[7:0]	0x51	RW		
lens_rx	C	21	[7:0]	0x00	RW		Lens shading center control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
lens_ry	C	22	[7:0]	0x00	RW		
lens_g1x	C	23	[7:0]	0x00	RW		
lens_g1y	C	24	[7:0]	0x00	RW		
lens_g2x	C	25	[7:0]	0x00	RW		
lens_g2y	C	26	[7:0]	0x00	RW		
lens_bx	C	27	[7:0]	0x00	RW		
lens_by	C	28	[7:0]	0x00	RW		
lens_gainr	C	1D	[7:0]	0x00	RW	aev	R gain for lens shading
lens_gaing1	C	1E	[7:0]	0x02	RW	aev	G1 gain for lens shading
lens_gaing2	C	1F	[7:0]	0x02	RW	aev	G2 gain for lens shading
lens_gainb	C	20	[7:0]	0x00	RW	aev	B gain for lens shading

White Balance Gain

WB gain is applied to images to remove the unrealistic color coming from different color temperature. Proper application of WB results in objects which appear white in person are displayed white in the output image.

Table 36 shows registers relevant to WB gain

Table 36 Register Table - White balance gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
awb_en	C	04	[6]	1'b1	RW	aev	AWB gain multification enable 1'b0 : disable 1'b1 : enable
wb_rgain_h	D	1B	[0]	0x00	RW	aev	
wb_rgain_l	D	1C	[7:0]	0x5D	RW	aev	
wb_ggain_h	D	1D	[0]	0x00	RW	aev	White balance gain
wb_ggain_l	D	1E	[7:0]	0x40	RW	aev	
wb_bgain_h	D	1F	[0]	0x00	RW	aev	
wb_bgain_l	D	20	[7:0]	0x5E	RW	aev	

Edge Enhancement

Edge enhancement function controls the sharpness of input image. The function is enabled by setting edge_en = 1’b1. Control factors for edge enhancement are edge gain, edge threshold, and edge maximum value.

- Edge gain
  Edge is intensified directly by setting high edge gain values. edge_gain, ec_pgain and ec_mgain affects positive edge gain and negative edge gain respectively.

- Edge threshold
  Threshold can be set to exclude edge with certain level to be excluded from edge enhancement process. Edge value smaller than dark_ec_pth are excluded from the process for positive edge. In similar fashion, edge value smaller than dark_ec_mth are excluded from the process for negative edge.

- Edge Max. value
  After edge threshold evaluation, maximum value clamping is proceeded. Maximum edge value for positive edge is dark_ec_pmax and for negative edge is dark_ec_mmax.

Table 37 shows registers relevant to edge enhancement functions.

Table 37 Register Table - Edge enhancement

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
edge_en	C	05	[3]	1'b1	RW	aev	Edge enhancement enable 1'b0 : disable 1'b1 : enable
edge_gain_lf	D	F4	[7:0]	0x30	RW	aev	Edge gain
edge_gain_ghf	D	F8	[7:0]	0x18	RW	aev	Edge gain ghf
edge_gain_ehf	D	FC	[7:0]	0x00	RW	aev	Edge gain ehf
ec_pgain	C	30	[7:0]	0x80	RW		Positive edge clamp gain
ec_mgain	C	31	[7:0]	0xFF	RW		Negative edge clamp gain
dark_ec_pth	D	68	[7:0]	0x04	RW	aev	Positive edge clamp threshold
dark_ec_mth	D	6C	[7:0]	0x04	RW	aev	Negative edge clamp threshold
dark_ec_pmax	D	70	[7:0]	0x7F	RW	aev	Max. positive edge clamp
dark_ec_mmax	D	74	[7:0]	0x7F	RW	aev	Max. negative edge clamp

Color Correction (CCR)

CCR function utilizes 3 by 3 matrix multiplication to correct RGB color. dark_ccr register reduces the effectiveness of CCR. As dark_ccr value increases, degree of CCR decreases.

$$\begin{bmatrix} R` \\ G` \\ B` \end{bmatrix} = \begin{bmatrix} ccr\_m11 & ccr\_m12 & ccr\_m13 \\ ccr\_m21 & ccr\_m22 & ccr\_m23 \\ ccr\_m31 & ccr\_m32 & ccr\_m33 \end{bmatrix} X \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Figure 32 CCR matrix

Table 38 shows registers relevant to CCR functions.

Table 38 Register Table - CCR

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ccr_en	C	04	[1]	1b'1	RW	aev	Color correction enable 1'b0 : disable 1'b1 : enable
ccr_m11	C	33	[7:0]	0x2B	RW		Color correction matrix value
ccr_m12	C	34	[7:0]	0x84	RW		
ccr_m13	C	35	[7:0]	0x87	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ccr_m21	C	36	[7:0]	0x86	RW		
ccr_m22	C	37	[7:0]	0x37	RW		
ccr_m23	C	38	[7:0]	0x91	RW		
ccr_m31	C	39	[7:0]	0x83	RW		
ccr_m32	C	3A	[7:0]	0x9C	RW		
ccr_m33	C	3B	[7:0]	0x3F	RW		
dark_ccr	D	59	[7:0]	0x00	RW	aev	Darkness value for color correction

RGB Gamma

RGB gamma function performs non-linear operation on RGB color after CCR. RGB gamma function can configure two different gamma reference curves: gamma curve1 and gamma curve2. Depending on the dark_rgb_gm setting level, the system determines which curve to apply for RGB (refer to Figure 33). RGB gamma is enabled by setting rgbgm_en = 1'b1.

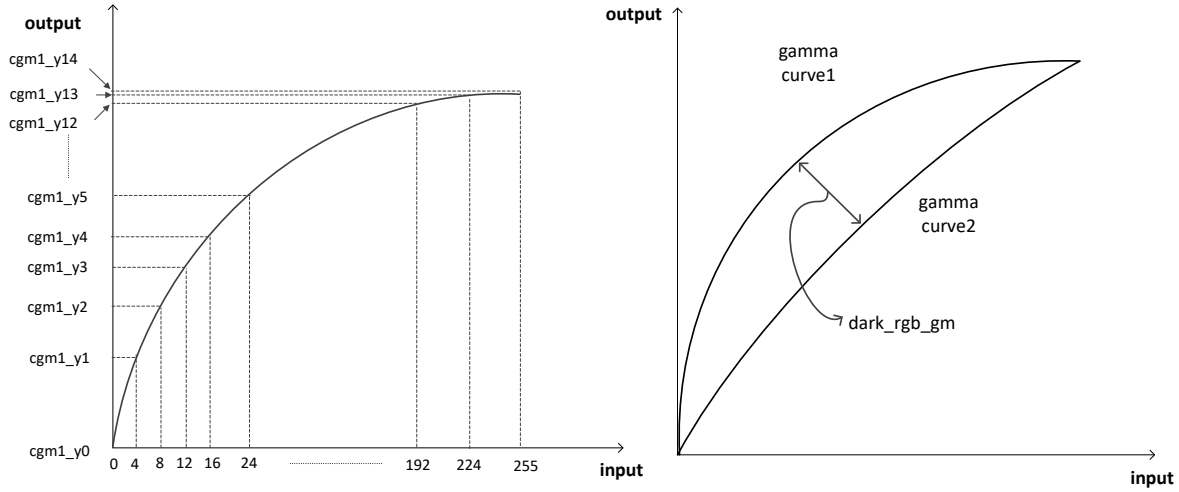


Figure 33 Gamma curve fitting of RGB gamma

Table 39 shows registers relevant to RGB gamma functions.

Table 39 Register Table - RGB gamma

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
rgbgm_en	C	05	[7]	1'b1	RW	aev	RGB gamma enable 1'b0 : disable 1'b1 : enable
cgm1_y0	C	5B	[7:0]	0x00	RW		Gamma curve reference1 for RGB gamma
cgm1_y1	C	5C	[7:0]	0x0F	RW		
cgm1_y2	C	5D	[7:0]	0x26	RW		
cgm1_y3	C	5E	[7:0]	0x37	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cgm1_y4	C	5F	[7:0]	0x43	RW		
cgm1_y5	C	60	[7:0]	0x54	RW		
cgm1_y6	C	61	[7:0]	0x62	RW		
cgm1_y7	C	62	[7:0]	0x77	RW		
cgm1_y8	C	63	[7:0]	0x88	RW		
cgm1_y9	C	64	[7:0]	0xA4	RW		
cgm1_y10	C	65	[7:0]	0xBB	RW		
cgm1_y11	C	66	[7:0]	0xCF	RW		
cgm1_y12	C	67	[7:0]	0xE0	RW		
cgm1_y13	C	68	[7:0]	0xF1	RW		
cgm1_y14	C	69	[7:0]	0xFF	RW		
cgm2_y0	C	6A	[7:0]	0x00	RW		
cgm2_y1	C	6B	[7:0]	0x07	RW		
cgm2_y2	C	6C	[7:0]	0x0D	RW		
cgm2_y3	C	6D	[7:0]	0x13	RW		
cgm2_y4	C	6E	[7:0]	0x18	RW		
cgm2_y5	C	6F	[7:0]	0x22	RW		
cgm2_y6	C	70	[7:0]	0x2C	RW		
cgm2_y7	C	71	[7:0]	0x3E	RW		Gamma curve reference2 for RGB gamma
cgm2_y8	C	72	[7:0]	0x4F	RW		
cgm2_y9	C	73	[7:0]	0x6F	RW		
cgm2_y10	C	74	[7:0]	0x8E	RW		
cgm2_y11	C	75	[7:0]	0xAC	RW		
cgm2_y12	C	76	[7:0]	0xC8	RW		
cgm2_y13	C	77	[7:0]	0xE4	RW		
cgm2_y14	C	78	[7:0]	0xFF	RW		
dark_rgb_gm	D	55	[7:0]	0x00	RW	aev	Darkness value for RGB gamma

De-color

De-color function reduces chroma level and is enabled by setting dc_en = 1’b1. High dark_dc level results in achromatic color. The maximum value of dark_dc is 0x3F.

Table 40 shows registers relevant to decolor functions.

Table 40 Register Table - De-color

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
dc_en	C	0A	[2]	1'b1	RW	aev	De-color enable 1'b0 : disable 1'b1 : enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
dark_dc	D	7A	[7:0]	0x00	RW	aev	De-color component

Y Gamma

Y gamma function performs non-linear operation on Y component. Y gamma function can configure two different gamma reference curves: gamma curve1 and gamma curve2. Depending on the dark_y_gm setting level, the system determines which curve to apply for Y (refer to Figure 34). Y gamma is enabled by setting ygm_en = 1'b1.

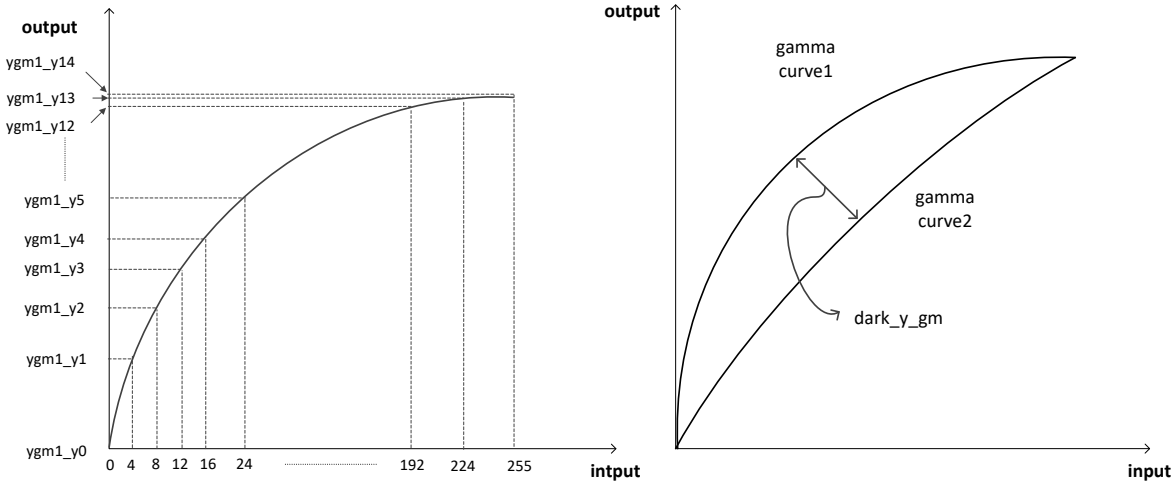


Figure 34 Gamma curve fitting of Y gamma

Table 41 shows registers relevant to Y gamma functions.

Table 41 Register Table - Y Gamma

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ygm_en	C	05	[6]	1'b1	RW	aev	Y gamma enable 1'b0 : disable 1'b1 : enable
ygm1_y0	C	3D	[7:0]	0x00	RW		Y gamma1 curve reference
ygm1_y1	C	3E	[7:0]	0x0C	RW		
ygm1_y2	C	3F	[7:0]	0x20	RW		
ygm1_y3	C	40	[7:0]	0x2F	RW		
ygm1_y4	C	41	[7:0]	0x3A	RW		
ygm1_y5	C	42	[7:0]	0x4B	RW		
ygm1_y6	C	43	[7:0]	0x58	RW		
ygm1_y7	C	44	[7:0]	0x6D	RW		
ygm1_y8	C	45	[7:0]	0x7F	RW		
ygm1_y9	C	46	[7:0]	0x9C	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ygm1_y10	C	47	[7:0]	0xB4	RW		
ygm1_y11	C	48	[7:0]	0xCA	RW		
ygm1_y12	C	49	[7:0]	0xDD	RW		
ygm1_y13	C	4A	[7:0]	0xEF	RW		
ygm1_y14	C	4B	[7:0]	0xFF	RW		
ygm2_y0	C	4C	[7:0]	0x00	RW		
ygm2_y1	C	4D	[7:0]	0x11	RW		
ygm2_y2	C	4E	[7:0]	0x1B	RW		
ygm2_y3	C	4F	[7:0]	0x23	RW		
ygm2_y4	C	50	[7:0]	0x2A	RW		
ygm2_y5	C	51	[7:0]	0x37	RW		
ygm2_y6	C	52	[7:0]	0x42	RW		
ygm2_y7	C	53	[7:0]	0x56	RW		Y gamma2 curve reference
ygm2_y8	C	54	[7:0]	0x68	RW		
ygm2_y9	C	55	[7:0]	0x87	RW		
ygm2_y10	C	56	[7:0]	0xA3	RW		
ygm2_y11	C	57	[7:0]	0xBC	RW		
ygm2_y12	C	58	[7:0]	0xD4	RW		
ygm2_y13	C	59	[7:0]	0xEA	RW		
ygm2_y14	C	5A	[7:0]	0xFF	RW		
dark_y_gm	D	51	[7:0]	0x00	RW	aev	Darkness value for Y gamma

Contrast

Contrast function performs linear operation on Y component. y_cont_th2 acts as the reference point of linear function, and y_cont_slope2 determines the linear function's slope.

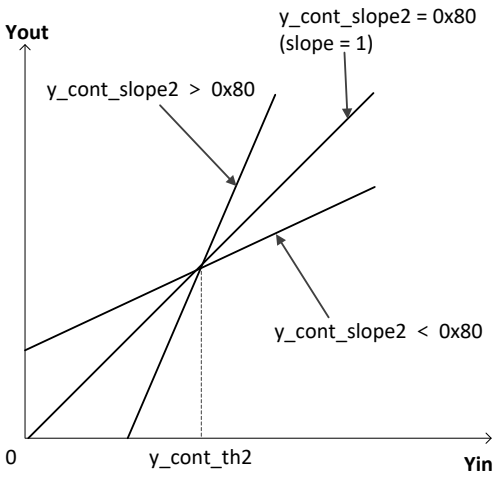


Figure 35 ISP Contrast control

Table 42 shows registers relevant to contrast functions.

Table 42 Register Table - Contrast

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
y_cont_th2	D	9A	[7:0]	0x80	RW	aev	X-axis standard for contrast line
y_cont_slope2	D	9E	[7:0]	0x40	RW	aev	Slope for contrast line

Color Saturation

Color saturation functions performs 2 by 2 matrix operation on chroma domain (Cb/Cr) to adjust hue and saturation. user_cs register is additional multiplication coefficient parameter for cs11 and cs22 components

$$\begin{bmatrix} Cb` \\ Cr` \end{bmatrix} = user\_cs \begin{bmatrix} cs11 & cs12 \\ cs21 & cs22 \end{bmatrix} X \begin{bmatrix} Cb \\ Cr \end{bmatrix}$$

Figure 36 Color saturation matrix

Table 43 shows registers relevant to color saturation functions.

Table 43 Register Table - Color saturation

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cs11	C	80	[7:0]	0x25	RW	aev	Color saturation matrix value
cs12	C	81	[7:0]	0x00	RW	aev	
cs21	C	82	[7:0]	0x00	RW	aev	
cs22	C	83	[7:0]	0x25	RW	aev	
user_cs	D	19	[7:0]	0x38	RW		User color saturation gain

Privacy Window

A privacy window is a function that covers a user's desired area with a specific color. When prvc_en = 1'b1, it is possible to control the privacy zone by setting prvc_wx1 / x2 / y1 / y2 as shown in << ISP_prvc_win >>. The color of the privacy window can be controlled by combining prvc_y / cb / cr. Figure 37 shows the privacy window according to the prvc_wx1 / x2 / y1 / y2 setting.

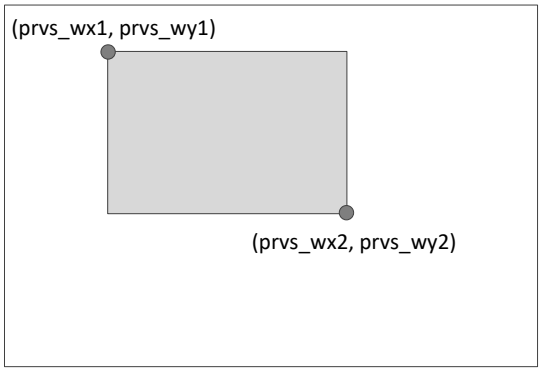


Figure 37 ISP privacy window

Table 44 is a list of registers related to the privacy window function.

Table 44 Register Table - privacy window

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
prvc_en	C	08	[3]	1'b0	RW	aev	Privacy mode enable
prvc_wx1_h	C	A0	[1:0]	0x00	RW		Privacy window start point control
prvc_wx1_l	C	A1	[7:0]	0x01	RW		
prvc_wx2_h	C	A2	[1:0]	0x02	RW		
prvc_wx2_l	C	A3	[7:0]	0x80	RW		
prvc_wy1_h	C	A4	[1:0]	0x00	RW		
prvc_wy1_l	C	A5	[7:0]	0x01	RW		
prvc_wy2_h	C	A6	[1:0]	0x00	RW		
prvc_wy2_l	C	A7	[7:0]	0xF0	RW		
prvc_y	C	A8	[7:0]	0x00	RW		Privacy window color control
prvc_cb	C	A9	[7:0]	0x80	RW		
prvc_cr	C	AA	[7:0]	0x80	RW		

Auto Exposure Control

AE Auto/Manual Mode Control

There are auto mode and manual mode in AE operation mode. Normally, it operates in auto mode. Auto/manual mode operates as follows according to exposure_mode [1:0] setting.

- exposure_mode[1:0] = 2'b00(auto mode)
  The exposure value changes according to the image characteristic. Inttime, globalgain, and digitalgain are calculated by the exposure value.
- exposure_mode[1:0] = 2'b01(manual1 : exposure control)
  The user can set the exposure directly. Inttime, globalgain, and digitalgain are calculated by the exposure value.
- exposure_mode[1:0] = 2'b10(manual2 : external gain control)
  The applied inttime corresponds to ext_inttime, and the applied globalgain corresponds to ext_glbg. User can set ext_inttime, ext_glbg directly.
- exposure_mode[1:0] = 2'b11(manual3 : inttime, gain control)
  User directly controls inttime, globalgain, and digitalgain.

Table 45 Register Table - AE manual

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
auto_off	C	8B	[7:0]	0x00	RW		Auto off (MCU off)
exposure mode	E	04	[1:0]	2'b00	RW	autov	Exposure mode selection 2'b00 : auto mode 2'b01 : manual1 (exposure write) 2'b10 : manual2 (ext_inttime, ext_glbgain write) 2'b11 : manual3 (inttime, globalgain write)
exposure_t	E	27	[7:0]	0x00	RW	autov	Exposure value
exposure_h	E	28	[7:0]	0x01	RW	autov	
exposure_m	E	29	[7:0]	0x40	RW	autov	
exposure_l	E	2A	[7:0]	0x00	RW	autov	
ext_inttime_h	E	22	[7:0]	0x00	RW	autov	Manual integration time @ external AE mode
ext_inttime_m	E	23	[7:0]	0x80	RW	autov	
ext_inttime_l	E	24	[7:0]	0x00	RW	autov	
ext_glbg_h	E	25	[7:0]	0x01	RW	autov	Manual analog gain @ external AE mode
ext_glbg_l	E	26	[7:0]	0x00	RW	autov	
inttime_h	B	BC	[7:0]	0x01	RW	aev	Integration time (line)
inttime_m	B	BD	[7:0]	0x40	RW	aev	
inttime_l	B	BE	[7:0]	0x00	RW	aev	Integration time (column)
globalgain	B	BF	[7:0]	0x00	RW	aev	Analog gain
digitalgain	B	C0	[7:0]	0x40	RW	aev	Digital gain

AE Window Setting

The AE window is divided into AE_window1, AE_windiw2, AE_windiw3, AE_window4, and AE_windowC areas(refer to Figure 38). The user can view the AE window as an output image by setting win_show[1] to 1'b1.

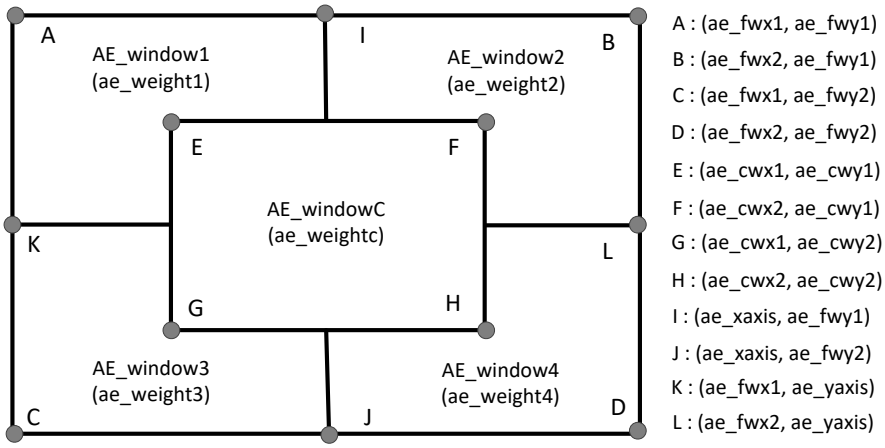


Figure 38 AE window setting

Table 46 Register Table - AE window setting

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
win_show	C	08	[7:6]	2'b00	RW	aev	win_show[1] : ae window show enable 1'b0 : disable 1'b1 : enable win_show[0] : awb window show enable 1'b0 : disable 1'b1 : enable
ae_fwx1_h	C	B3	[1:0]	0x00	RW		AE window control
ae_fwx1_l	C	B4	[7:0]	0x01	RW		
ae_fwx2_h	C	B5	[1:0]	0x03	RW		
ae_fwx2_l	C	B6	[7:0]	0xC0	RW		
ae_fwy1_h	C	B7	[1:0]	0x00	RW		
ae_fwy1_l	C	B8	[7:0]	0x01	RW		
ae_fwy2_h	C	B9	[1:0]	0x01	RW		
ae_fwy2_l	C	BA	[7:0]	0xE0	RW		
ae_cwx1_h	C	BB	[1:0]	0x01	RW		
ae_cwx1_l	C	BC	[7:0]	0x41	RW		
ae_cwx2_h	C	BD	[1:0]	0x02	RW		
ae_cwx2_l	C	BE	[7:0]	0x80	RW		
ae_cwy1_h	C	BF	[1:0]	0x00	RW		
ae_cwy1_l	C	C0	[7:0]	0xA1	RW		
ae_cwy2_h	C	C1	[1:0]	0x01	RW		
ae_cwy2_l	C	C2	[7:0]	0x40	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ae_xaxis_h	C	C3	[1:0]	0x01	RW		
ae_xaxis_l	C	C4	[7:0]	0xE1	RW		
ae_yaxis_h	C	C5	[1:0]	0x00	RW		
ae_yaxis_l	C	C6	[7:0]	0xF1	RW		

Auto White Balance Control

AWB Auto/Manual Mode Control

There are auto mode and manual mode in AWB operation mode. Normally, it operates in auto mode. Auto/manual mode operates as follows according to wb_mode setting.

- wb_mode = 1'b0(auto mode)
  The AWB block calculates the WB gain to match the white balance. WB gain is stored in wb_rgain_h to wb_bgain_l.

- wb_mode = 1'b1(manual mode)
  The user can adjust the WB gain by directly writing wb_rgain_h to wb_bgain_l.

Wb_gratio adjusts the G gain value among the WB gains. The default value is 0x80. As the data is written more than 0x80, the image has a greenish characteristic.

Table 47 Register Table - AWB Manual

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
wb mode	E	04	[2]	1'b0	RW	autov	White blance mode selection 1'b0 : auto mode 1'b1 : manual mode using wb_rgain_h ~ wb_bgain_l
wb_rgain_h	D	1B	[0]	0x00	RW	aev	White balance gain @ wb_manual = 00h
wb_rgain_l	D	1C	[7:0]	0x5D	RW	aev	
wb_ggain_h	D	1D	[0]	0x00	RW	aev	
wb_ggain_l	D	1E	[7:0]	0x40	RW	aev	
wb_bgain_h	D	1F	[0]	0x00	RW	aev	
wb_bgain_l	D	20	[7:0]	0x5E	RW	aev	
wb_gratio	D	5B	[7:0]	0x80	RW		wb_ggain ratio

AWB Window Setting

The AWB window setting controls the area to be applied to the AWB calculation(refer to Figure 39). The user can view the AWB window as an output image by setting win_show[0] to 1'b1.

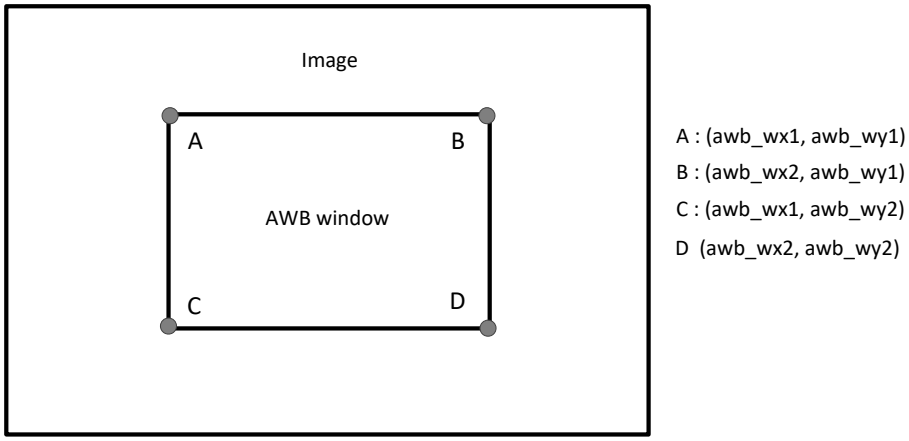


Figure 39 AWB window setting

Table 48 Register Table - AWB window

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
win_show	C	08	[7:6]	2'b00	RW	aev	win_show[1] : ae window show enable 1'b0 : disable 1'b1 : enable win_show[0] : awb window show enable 1'b0 : disable 1'b1 : enable
awb_wx1_h	C	C7	[1:0]	0x00	RW		AWB window control
awb_wx1_l	C	C8	[7:0]	0x01	RW		
awb_wx2_h	C	C9	[1:0]	0x03	RW		
awb_wx2_l	C	CA	[7:0]	0xC0	RW		
awb_wy1_h	C	CB	[1:0]	0x00	RW		
awb_wy1_l	C	CC	[7:0]	0x01	RW		
awb_wy2_h	C	CD	[1:0]	0x01	RW		
awb_wy2_l	C	CE	[7:0]	0xE0	RW		

TV Encoder

Encoder Mode

PC1058D supports NTSC, PAL mode (TV mode). In detail, there are NTSC-M, NTSC-J, PAL-M, PAL-NC, PAL-D (B, G, H, I and N), PAL-N and NTSC-4.43.

Table 49 Register Table - Encoder mode

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_mode	H	B7	[1:0]	0xx	RW		Encoder mode

Horizontal Timing Control

User can control setup time, sync rising / falling timing and active data rising / falling timing according to the situation.

- Setup time
  The setup time representing the black level can be set between 0x00 and 0x1F in pclk units by setting setup_w. Figure 40 shows the horizontal time, including the setup time.

- Hsync rising(falling) and data rising(falling)
  By setting sync_rising, sync rising/falling time can be controlled. Sync_rising has a range of 0x00 to 0x0F. The unit of sync_rising is pclk.

The rising/falling time of horizontal active data start/stop is controlled by setting encdat_rising. Encdat_rising has a range of 0x00 to 0x0F. The unit of encdat_rising is pclk.

Figure 40 shows horizontal timeing including sync rising/falling and data rising/falling.

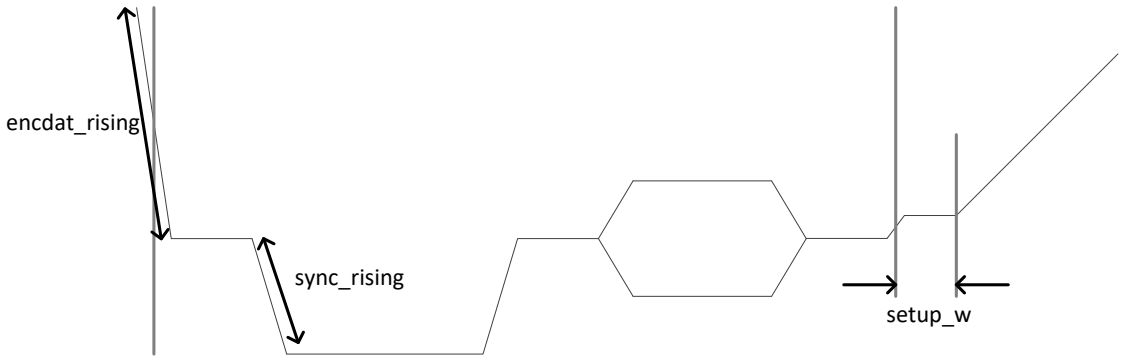


Figure 40 Horizontal timing

Table 50 Register Table - Horizontal timing

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
setup_w	H	A9	[4:0]	0x07	RW		Setup time width

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_rising	H	AF	[3:0]	0x01	RW		Horizontal sync rising(falling) time control
encdat_rising	H	F2	[3:0]	0x01	RW		Edge of the line blanking pulse rising(falling) time control

Subcarrier Frequency(Color Burst)

The TV composite signal is generated by using the modulation that sends the luminance component to the main and the chrominance component to the subcarrier. To decode the frequency and phase of the subcarrier in the decoder, the TV encoder sends a subcarrier signal to a specific section of the line blank. A color burst refers to a subcarrier signal present in a specific section of a line blank. The subcarrier may be different depending on the TV mode. By setting enc_scfreq, you can set the subcarrier for TV mode. The user can set the color burst start position, duration, burst slope, and subcarrier phase offset to suit the situation. Figure 41 shows the burst start position, duration, and burst slope control.

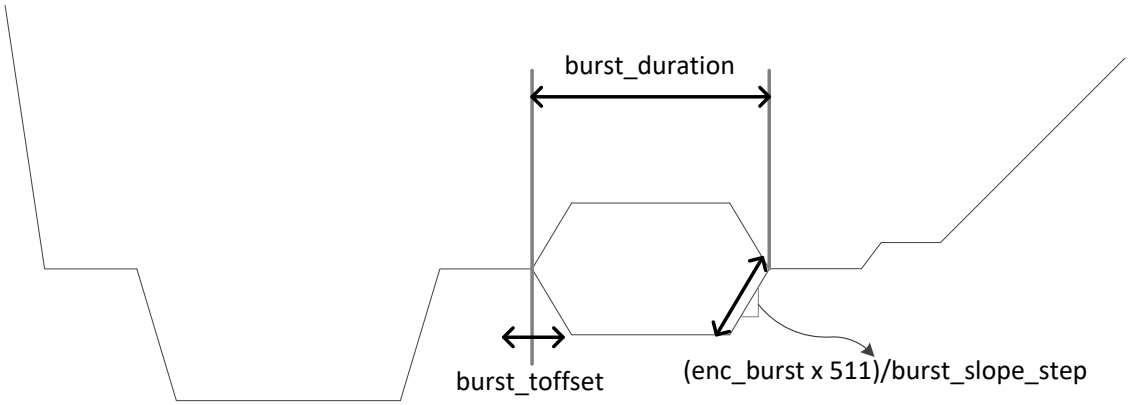


Figure 41 Burst timing

- burst_duration
  burst_duration[7]=1'b0 : burst duration = reference burst duration + burst_duration[6:0]
  burst_duration[7]=1'b1 : burst duration = reference burst duration - burst_duration[6:0]

- burst_toffset
  burst_toffset[7]=1'b0 : burst start point = reference burst start point + burst_toffset[6:0]
  burst_toffset[7]=1'b1 : burst start point = reference burst start point - burst_toffset[6:0]

- enc_SCH_offset
  The TV encoder controls the subcarrier phase offset based on the first line's sync falling(at the 50% amplitude point of the horizontal leading edge). Figure 42 shows control of the subcarrier phase offset.
  Example of subcarrier phase(sync rising to subcarrier) setting
  enc_SCH_offset=0x00000000 : 0^o
  enc_SCH_offset=0x40000000 : 90^o
  enc_SCH_offset=0x80000000 : 180^o
  enc_SCH_offset=0xC0000000 : 270^o

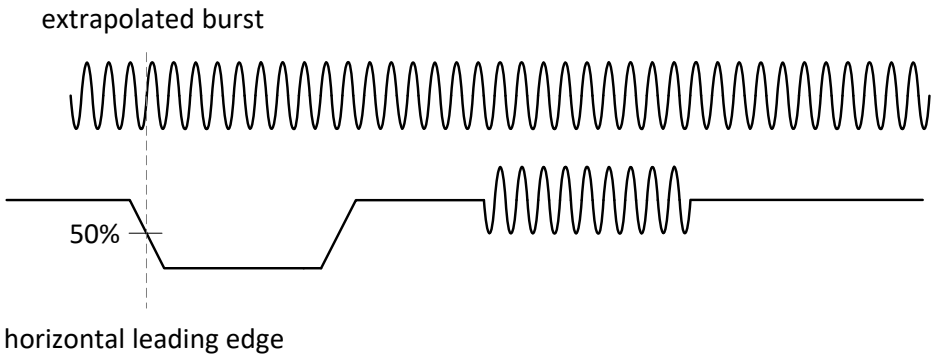


Figure 42 Subcarrier phase offset control

Table 51 Register Table - Burst timing

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
burst_duration	H	AB	[7:0]	0x00	RW		Burst duration
burst_slope_step	H	AC	[7:0]	0x38	RW		burst rising(falling) slope control
enc_SCH_offset_T	H	E8	[7:0]	0x00	RW		SCH(subcarrier to horizontal) phase offset
enc_SCH_offset_H	H	E9	[7:0]	0x00	RW		
enc_SCH_offset_M	H	EA	[7:0]	0x00	RW		
enc_SCH_offset_L	H	EB	[7:0]	0x00	RW		
DAC_tp_period	H	EC	[7:0]	0x00	RW		DAC test pattern period
burst_toffset	H	ED	[7:0]	0x00	RW		Burst time offset
enc_scfreq	H	F3	[1:0]	0xx	RW		2'b00 : 3.579545 MHz for NTSC-M, NTSC-J 2'b01 : 4.43361875 MHz for PAL-(B, D, G, H, I, N) 2'b10 : 3.58205625 MHz for PAL-NC 2'b11 : 3.57561149 MHz for (M) PAL

Composite Level and Data Range

Each TV standard offers different levels of sync level, blank level, pedestal level, burst amplitude, and composite signal maximum level. So PC1058D is designed to be register controlled to meet each TV standard. The TV encoder uses an 11-bit data width to internally generate a composite signal and clamps it to send 10-bit data to the DAC. The user must control the min / max and Y / C range of the composite signal for clamping. Figure 43 and Figure 44 show composite signal level and data (Y / C) ranges, respectively.

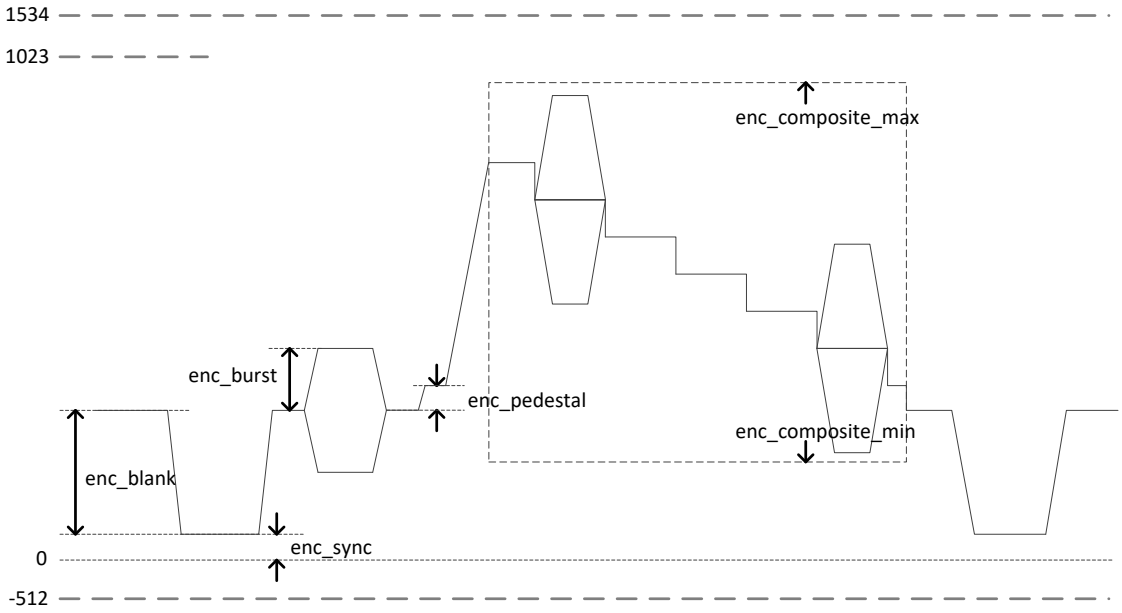


Figure 43 Composite level

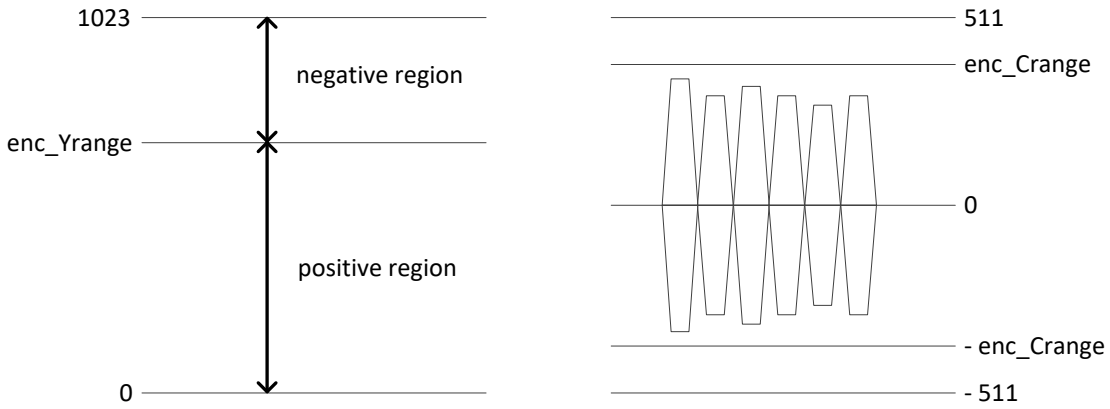


Figure 44 Data range

Table 52 Register Table - Composite level and data range

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_sync	H	B8	[7:0]	0x10	RW		composite sync level
enc_blankH	H	B9	[7:0]	0x00	RW		Composite blank level
enc_blankL	H	BA	[7:0]	0xx	RW		
enc_pedestal	H	BB	[7:0]	0xx	RW		Composite pedestal level
enc_burst	H	BC	[7:0]	0xx	RW		Burst amplitude
enc_Ygain	H	BD	[7:0]	0xx	RW		Y convergence gain from YCbCr to YUV
enc_Ugain	H	BE	[7:0]	0xx	RW		U convergence gain from YCbCr to YUV
enc_Vgain	H	BF	[7:0]	0xx	RW		V convergence gain from YCbCr to YUV

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_Yrange_H	H	C0	[7:0]	0x03	RW		Max. luminance
enc_Yrange_L	H	C1	[7:0]	0x20	RW		
enc_Crange_H	H	C2	[7:0]	0x01	RW		Max. amplitudes of chrominance
enc_Crange_L	H	C3	[7:0]	0xx	RW		
enc_chroma_max_H	H	C4	[7:0]	0x03	RW		Maximum chrominance of composite output
enc_chroma_max_L	H	C5	[7:0]	0xx	RW		
enc_chroma_min_H	H	C6	[7:0]	0x00	RW		Minimum chrominance of composite output
enc_chroma_min_L	H	C7	[7:0]	0xx	RW		

Color Kill

In low-light conditions where the IR LED is lit, the TV encoder input may be a black and white image with no color components. In this case, the TV encoder can make the chrominance range of the color burst and the active line zero in black and white mode. It can also be controlled manually.

Table 53 Register Table - Color kill

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_chroma_kill	H	9D	[3]	1'b0	RW		Composite chroma signal kill enable@led on(bw mode) 1'b0 : disable 1'b1 : enable
burst kill	A	8F	[1]	1'b0	RW		Composite color burst signal kill enable@led on(bw mode) 1'b0 : disable 1'b1 : enable
manual_chroma_kill	H	9D	[1]	1'b0	RW		Composite chroma signal manual kill enable 1'b0 : disable 1'b1 : enable
manual_burst_kill	H	9D	[0]	1'b0	RW		Composite color burst manual kill enable 1'b0 : disable 1'b1 : enable

GPO

When GPO (Genral Purpose Output) is used, user can output desired value to data pad.

GPO Using I2C

PC1058D can use D9 ~ D2 pad as GPO pad. To use the GPO function, the D9 to D2 pad must be enabled. If d_pad_selection is 1'b1, user can control output of D9~D2 pad by setting d9~d2_pad_manual.

Table 54 Register Table - I2C GPO control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
d9_pad_en	A	2E	[7]	1'b0	RW		D9 pad enable
d8_pad_en	A	2E	[6]	1'b0	RW		D8 pad enable
d7_pad_en	A	2E	[5]	1'b0	RW		D7 pad enable
d6_pad_en	A	2E	[4]	1'b0	RW		D6 pad enable
d5_pad_en	A	2E	[3]	1'b0	RW		D5 pad enable
d4_pad_en	A	2E	[2]	1'b0	RW		D4 pad enable
d3_pad_en	A	2E	[1]	1'b0	RW		D3 pad enable
d2_pad_en	A	2E	[0]	1'b0	RW		D2 pad enable
d9_pad_manual	A	2F	[7]	1'b0	RW		D9 pad output set 1'b1 : High 1'b0 : Low
d8_pad_manual	A	2F	[6]	1'b0	RW		D8 pad output set 1'b1 : High 1'b0 : Low
d7_pad_manual	A	2F	[5]	1'b0	RW		D7 pad output set 1'b1 : High 1'b0 : Low
d6_pad_manual	A	2F	[4]	1'b0	RW		D6 pad output set 1'b1 : High 1'b0 : Low
d5_pad_manual	A	2F	[3]	1'b0	RW		D5 pad output set 1'b1 : High 1'b0 : Low
d4_pad_manual	A	2F	[2]	1'b0	RW		D4 pad output set 1'b1 : High 1'b0 : Low
d3_pad_manual	A	2F	[1]	1'b0	RW		D3 pad output set 1'b1 : High 1'b0 : Low
d2_pad_manual	A	2F	[0]	1'b0	RW		D2 pad output set 1'b1 : High 1'b0 : Low
d_pad_selection	A	29	[0]	1'b0	RW		GPO enable 1'b0 : GPO disable 1'b1 : D9~D2 pad are correspond to d9~d2_pad_manual

Electrical Characteristics

PC1058D does not have tolerant input pads. The input signal must have HVDD power level for stable operation. If the power of input signal is higher than the recommended level, leakage current may flow via short circuit path in the input pads.

DC Characteristics(TBD)

Absolute maximum ratings [1]
AVDD supply voltage : -0.3 [V] to 4.5 [V]
HVDD supply voltage : -0.3 [V] to 4.5 [V]
CVDD supply voltage : -0.3 [V] to 4.5 [V]
DVDD supply voltage(using external LDO) : -0.3 [V] to 2.5 [V]
DC voltage at any input pin : -0.3 [V] to HVDD+0.3 [V]
DC voltage at any output pin : -0.3 [V] to HVDD+0.3 [V]
Storage temperature : -40 [^{o}C] to + 125 [^{o}C]

Table 55 DC characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
AVDD	Analog voltage relative to GND(AGND) level	2.97	3.3	3.63	[V]
HVDD	High VDD(HVDD) voltage relative to GND(DGND) level	2.97	3.3	3.63	[V]
CVDD	DAC VDD(CVDD) voltage relative to GND(CGND) level	2.97	3.3	3.63	[V]
I_{DDD}	HVDD=3.3 [V]	42.0@NTSC 42.3@PAL	46.0@NTSC 46.7@PAL	48.3@NTSC 51.0@PAL	[mA]
	AVDD=3.3 [V]	12.0	12.7	13.3	
	CVDD=3.3 [V]	32.0	32.7	33.3	
I_{DDS}	Standby supply current @ all = 3.3 [V]	126.7	170.7	201.7	[uA]
V_{IL1}	Input voltage low level	-0.3	-	HVDD*0.3	[V]
V_{IH1}	Input voltage high level	HVDD*0.7	-	4	[V]
V_{IL2}	Input voltage low level for rClk, rData.	-0.3	-	HVDD*0.3	[V]
V_{IH2}	Input voltage high level for rClk, rData	HVDD*0.7	-	4	[V]
C_{IN}	Input pin capacitance	-	-	10	[pF]
V_{OL1}	Output voltage low	-	-	0.2	[V]
V_{OH1}	Output voltage high	HVDD-0.2	-	-	[V]
V_{OL2}	Output voltage low level for rClk, rData.	-	-	0.2	[V]
V_{OH2}	Output voltage high level for rData.	HVDD-0.2	-	-	[V]
I_{IN}	Input leakage current	-	0.005	1	[uA]
I_{OT}	Output leakage current	-	0.005	1	[uA]

[1]Excessive stresses may cause permanent damage to the device.

AC Characteristics(TBD)

test conditon : input clock = 27Mhz, AVDD/HVDD/CVDD=3.3V, using internal LDO, 25 ^{o}C

Table 56 2-wire serial interface characteristics

Symbol	Descriptions	Min	Max	Unit
fSCLK	2-wire serial interface Clock frequency	-	400	kHz
Tic	2-wire serial interface Clock period	2.5	-	us
Ticl	2-wire serial interface Clock low level width	1.66	-	us
Tich	2-wire serial interface Clock high level width	0.83	-	us
Tiss	setup time for start condition	0.83	-	us
Tihs	hold time for start condition	0.83	-	us
Tisd	setup time for input data	266	-	ns
Tihd	hold time for input data	0	-	ns
Tisp	setup time for stop condition	0.83	-	us
Tbuf	bus free time between a stop and a new start condition	1.66	-	us
Toaa	delay from SCL falling edge to output data transition	-	354	ns
Tr	10% to 90% rising time for SCL/SDA (load : 10pF)	139	336	ns
Tf	90% to 10% falling time for SCL/SDA (load : 10pF)	4.3	5.8	ns
Rp	SCL, SDA pull-up resistor	1	TBD	kΩ

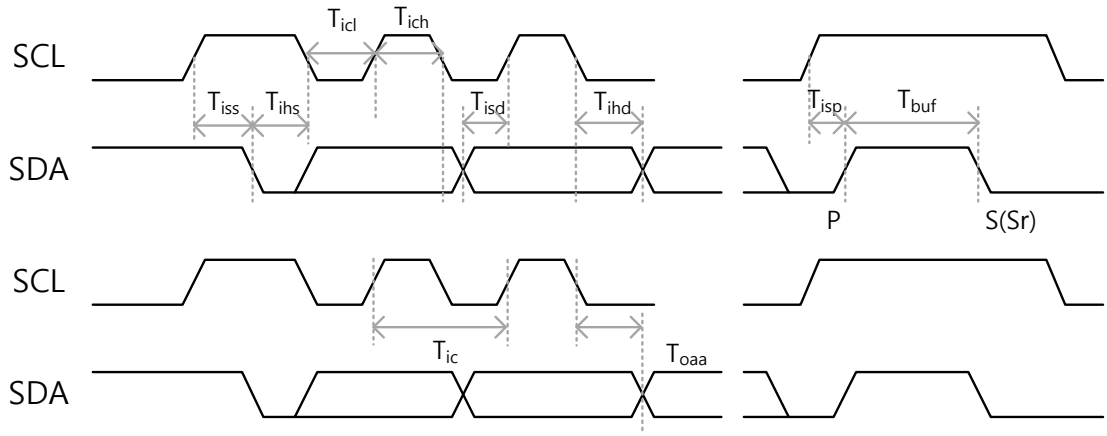


Figure 45 Timing diagram of SCL and SDA

Table 57 SPI timing

Symbol	parameter	Min	typ	Max	Unit
Twh	SCK high time	0.5	-	-	SPI clk
Twl	SCK low time	0.5	-	-	SPI clk
Tcs	CS high time	7	-	-	SPI clk
Tcss	CS setup time	1.5	-	-	SPI clk
Tcsh	CS hold time	1	-	-	SPI clk
Tsu	Data in setup time	7	-	-	ns
Th	Data in hold time	9.5	-	-	ns
Tv	Output valid		-	0.5	SPI clk
Tho	Output hold time	0.5	-	-	SPI clk
tdis	Output disable time		-	0	SPI clk

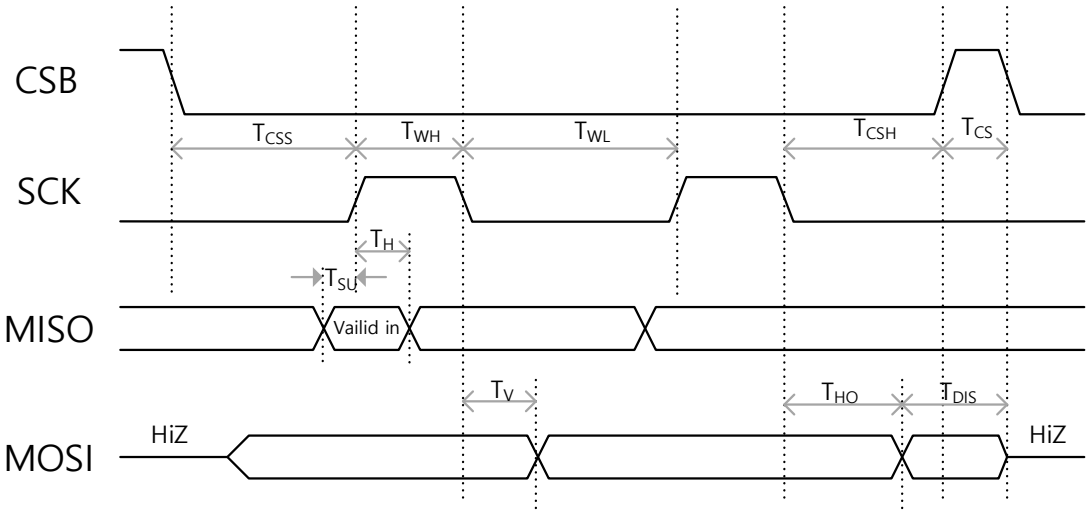


Figure 46 SPI timing diagram

Register Map

Table 58 Register Table - Group A

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bank	A	03	[7:0]	0x00	RW		Register group selector
chip_mode	A	04	[1:0]	0xx	RW	aev	chip mode selection(NTSC, PAL, 960H)
framewidth_h	A	06	[3:0]	0xx	RW	aev	Framewidth
framewidth_l	A	07	[7:0]	0xx	RW	aev	
fd_fheight_a_h	A	08	[4:0]	0x02	RW	aev	Frameheight
fd_fheight_a_l	A	09	[7:0]	0xx	RW	aev	
fd_fheight_b_h	A	0A	[4:0]	0x02	RW	aev	
fd_fheight_b_l	A	0B	[7:0]	0xx	RW	aev	
windowx1_h	A	0C	[1:0]	0x00	RW	aev	Window
windowx1_l	A	0D	[7:0]	0x01	RW	aev	
windowy1_h	A	0E	[1:0]	0x00	RW	aev	
windowy1_l	A	0F	[7:0]	0x01	RW	aev	
windowx2_h	A	10	[1:0]	0x03	RW	aev	
windowx2_l	A	11	[7:0]	0xC0	RW	aev	
windowy2_h	A	12	[1:0]	0x01	RW	aev	
windowy2_l	A	13	[7:0]	0xE0	RW	aev	
vsyncstartrow_f0_h	A	14	[4:0]	0x00	RW	aev	Vsync generation
vsyncstartrow_f0_l	A	15	[7:0]	0x17	RW	aev	
vsyncstoprow_f0_h	A	16	[4:0]	0x01	RW	aev	
vsyncstoprow_f0_l	A	17	[7:0]	0xx	RW	aev	
vsyncstartrow_f1_h	A	18	[4:0]	0x01	RW	aev	
vsyncstartrow_f1_l	A	19	[7:0]	0xx	RW	aev	
vsyncstoprow_f1_h	A	1A	[4:0]	0x02	RW	aev	
vsyncstoprow_f1_l	A	1B	[7:0]	0xx	RW	aev	
vsynccolumn_h	A	1C	[3:0]	0x00	RW		
vsynccolumn_l	A	1D	[7:0]	0x02	RW		
clkdiv	A	25	[5:0]	0x28	RW	aev	Clock divider
strap_control	A	30	[7:0]	0xFF	RW		Strap control
pll_control1	A	4A	[7:0]	0x38	RW		PLL control
pll_ms	A	4D	[7:0]	0x03	RW		PLL division factor
pll_ns	A	4E	[7:0]	0x08	RW		PLL multiplication factor
flicker_control1	A	4F	[7:0]	0xx	RW		Flicker control
led_control1	A	8E	[7:0]	0x00	RW		LED control
led_lvth1	A	90	[7:0]	0x00	RW		LED control level th.1
led_lvth2	A	91	[7:0]	0x00	RW		LED control elvel th.2

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
led_frame	A	92	[7:0]	0x80	RW		LED frame control
mirs_pw	A	93	[7:0]	0x64	RW		mirs pulse width
mirs_pp	A	95	[7:0]	0xC8	RW		mirs pulse period control
mirs_cnt	A	96	[7:0]	0x01	RW		the number of mirs pulses control

Table 59 Register Table - Group B

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bayer_control_01	B	15	[7:0]	0x05	RW		Bayer control
bayer_control_02	B	16	[7:0]	0xFA	RW		
front_black_ref0	B	A0	[7:0]	0x00	RW		Front black control
front_black_ref1	B	A1	[7:0]	0x00	RW		
front_black_ref2	B	A2	[7:0]	0x00	RW		
front_black_ref3	B	A3	[7:0]	0x00	RW		
front_black_ref4	B	A4	[7:0]	0x00	RW		
front_black_ref5	B	A5	[7:0]	0x00	RW		
front_black_min	B	A6	[7:0]	0xFF	RW		
front_black_max	B	A7	[7:0]	0x7F	RW		
front_black	B	A8	[7:0]	0x00	RW	aev	
inttime_h	B	BC	[7:0]	0x01	RW	aev	Integration time (line)
inttime_m	B	BD	[7:0]	0x40	RW	aev	
inttime_l	B	BE	[7:0]	0x00	RW	aev	Integration time (column)
globalgain	B	BF	[7:0]	0x00	RW	aev	Analog gain
digitalgain	B	C0	[7:0]	0x40	RW	aev	Digital gain
real_led_data	B	D7	[7:0]		RO		Current CdS data

Table 60 Register Table - Group C

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
isp_func_2	C	06	[7:0]	0x00	RW	aev	Isp function control
isp_func_4	C	08	[7:0]	0x00	RW	aev	
format	C	29	[7:0]	0x00	RW	aev	Format control
ygm1_y0	C	3D	[7:0]	0x00	RW		Y gamma1 coefficient
ygm1_y1	C	3E	[7:0]	0x0C	RW		
ygm1_y2	C	3F	[7:0]	0x20	RW		
ygm1_y3	C	40	[7:0]	0x2F	RW		
ygm1_y4	C	41	[7:0]	0x3A	RW		
ygm1_y5	C	42	[7:0]	0x4B	RW		
ygm1_y6	C	43	[7:0]	0x58	RW		
ygm1_y7	C	44	[7:0]	0x6D	RW		
ygm1_y8	C	45	[7:0]	0x7F	RW		
ygm1_y9	C	46	[7:0]	0x9C	RW		
ygm1_y10	C	47	[7:0]	0xB4	RW		
ygm1_y11	C	48	[7:0]	0xCA	RW		
ygm1_y12	C	49	[7:0]	0xDD	RW		
ygm1_y13	C	4A	[7:0]	0xEF	RW		
ygm1_y14	C	4B	[7:0]	0xFF	RW		
ygm2_y0	C	4C	[7:0]	0x00	RW		Y gamma2 coefficient
ygm2_y1	C	4D	[7:0]	0x11	RW		
ygm2_y2	C	4E	[7:0]	0x1B	RW		
ygm2_y3	C	4F	[7:0]	0x23	RW		
ygm2_y4	C	50	[7:0]	0x2A	RW		
ygm2_y5	C	51	[7:0]	0x37	RW		
ygm2_y6	C	52	[7:0]	0x42	RW		
ygm2_y7	C	53	[7:0]	0x56	RW		
ygm2_y8	C	54	[7:0]	0x68	RW		
ygm2_y9	C	55	[7:0]	0x87	RW		
ygm2_y10	C	56	[7:0]	0xA3	RW		
ygm2_y11	C	57	[7:0]	0xBC	RW		
ygm2_y12	C	58	[7:0]	0xD4	RW		
ygm2_y13	C	59	[7:0]	0xEA	RW		
ygm2_y14	C	5A	[7:0]	0xFF	RW		
cgm1_y0	C	5B	[7:0]	0x00	RW		RGB gamma1 coefficient
cgm1_y1	C	5C	[7:0]	0x0F	RW		
cgm1_y2	C	5D	[7:0]	0x26	RW		
cgm1_y3	C	5E	[7:0]	0x37	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cgm1_y4	C	5F	[7:0]	0x43	RW		
cgm1_y5	C	60	[7:0]	0x54	RW		
cgm1_y6	C	61	[7:0]	0x62	RW		
cgm1_y7	C	62	[7:0]	0x77	RW		
cgm1_y8	C	63	[7:0]	0x88	RW		
cgm1_y9	C	64	[7:0]	0xA4	RW		
cgm1_y10	C	65	[7:0]	0xBB	RW		
cgm1_y11	C	66	[7:0]	0xCF	RW		
cgm1_y12	C	67	[7:0]	0xE0	RW		
cgm1_y13	C	68	[7:0]	0xF1	RW		
cgm1_y14	C	69	[7:0]	0xFF	RW		
cgm2_y0	C	6A	[7:0]	0x00	RW		RGB gamma2 coefficient
cgm2_y1	C	6B	[7:0]	0x07	RW		
cgm2_y2	C	6C	[7:0]	0x0D	RW		
cgm2_y3	C	6D	[7:0]	0x13	RW		
cgm2_y4	C	6E	[7:0]	0x18	RW		
cgm2_y5	C	6F	[7:0]	0x22	RW		
cgm2_y6	C	70	[7:0]	0x2C	RW		
cgm2_y7	C	71	[7:0]	0x3E	RW		
cgm2_y8	C	72	[7:0]	0x4F	RW		
cgm2_y9	C	73	[7:0]	0x6F	RW		
cgm2_y10	C	74	[7:0]	0x8E	RW		
cgm2_y11	C	75	[7:0]	0xAC	RW		
cgm2_y12	C	76	[7:0]	0xC8	RW		
cgm2_y13	C	77	[7:0]	0xE4	RW		
cgm2_y14	C	78	[7:0]	0xFF	RW		
y_weight	C	8D	[7:0]	0x40	RW	aev	Y weight
ycontrast	C	94	[7:0]	0x40	RW	aev	Dark Y contrast
ybrightness	C	98	[7:0]	0x00	RW	aev	Dark Y brightness
prvc_wx1_h	C	A0	[1:0]	0x00	RW		Privacy window size control
prvc_wx1_l	C	A1	[7:0]	0x01	RW		
prvc_wx2_h	C	A2	[1:0]	0x02	RW		
prvc_wx2_l	C	A3	[7:0]	0x80	RW		
prvc_wy1_h	C	A4	[1:0]	0x00	RW		
prvc_wy1_l	C	A5	[7:0]	0x01	RW		
prvc_wy2_h	C	A6	[1:0]	0x00	RW		
prvc_wy2_l	C	A7	[7:0]	0xF0	RW		
prvc_y	C	A8	[7:0]	0x00	RW		YCbCr of privacy window

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
prvc_cb	C	A9	[7:0]	0x80	RW		
prvc_cr	C	AA	[7:0]	0x80	RW		
ae_fwx1_h	C	B3	[1:0]	0x00	RW		AE full window X start position
ae_fwx1_l	C	B4	[7:0]	0x01	RW		
ae_fwx2_h	C	B5	[1:0]	0x03	RW		AE full window X stop position
ae_fwx2_l	C	B6	[7:0]	0xC0	RW		
ae_fwy1_h	C	B7	[1:0]	0x00	RW		AE full window Y start position
ae_fwy1_l	C	B8	[7:0]	0x01	RW		
ae_fwy2_h	C	B9	[1:0]	0x01	RW		AE full window Y stop position
ae_fwy2_l	C	BA	[7:0]	0xE0	RW		
ae_cwx1_h	C	BB	[1:0]	0x01	RW		AE center window X start position
ae_cwx1_l	C	BC	[7:0]	0x41	RW		
ae_cwx2_h	C	BD	[1:0]	0x02	RW		AE center window X stop position
ae_cwx2_l	C	BE	[7:0]	0x80	RW		
ae_cwy1_h	C	BF	[1:0]	0x00	RW		AE center window Y start position
ae_cwy1_l	C	C0	[7:0]	0xA1	RW		
ae_cwy2_h	C	C1	[1:0]	0x01	RW		AE center window Y stop position
ae_cwy2_l	C	C2	[7:0]	0x40	RW		
ae_xaxis_h	C	C3	[1:0]	0x01	RW		AE window X axis
ae_xaxis_l	C	C4	[7:0]	0xE1	RW		
ae_yaxis_h	C	C5	[1:0]	0x00	RW		AE window Y axis
ae_yaxis_l	C	C6	[7:0]	0xF1	RW		
awb_wx1_h	C	C7	[1:0]	0x00	RW		AWB window X start position
awb_wx1_l	C	C8	[7:0]	0x01	RW		
awb_wx2_h	C	C9	[1:0]	0x03	RW		AWB window X stop position
awb_wx2_l	C	CA	[7:0]	0xC0	RW		
awb_wy1_h	C	CB	[1:0]	0x00	RW		AWB window Y start position
awb_wy1_l	C	CC	[7:0]	0x01	RW		
awb_wy2_h	C	CD	[1:0]	0x01	RW		AWB window Y stop position
awb_wy2_l	C	CE	[7:0]	0xE0	RW		

Table 61 Register Table - Group D

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
user_cs	D	19	[7:0]	0x38	RW		User CS gain
wb_rgain_h	D	1B	[0]	0x00	RW	aev	Normalized white balance gain
wb_rgain_l	D	1C	[7:0]	0x5D	RW	aev	
wb_ggain_h	D	1D	[0]	0x00	RW	aev	
wb_ggain_l	D	1E	[7:0]	0x40	RW	aev	
wb_bgain_h	D	1F	[0]	0x00	RW	aev	
wb_bgain_l	D	20	[7:0]	0x5E	RW	aev	
dark_ccr	D	59	[7:0]	0x00	RW	aev	Dark color correction value
dark_y_gm	D	51	[7:0]	0x00	RW	aev	Dark Y gamma value
dark_rgb_gm	D	55	[7:0]	0x00	RW	aev	Dark RGB gamma value
wb_gratio	D	5B	[7:0]	0x80	RW		Gr/Gb ratio of white balance gain value
dark_ec_pth	D	68	[7:0]	0x04	RW	aev	Dark edge clamp plus threshold value
dark_ec_mth	D	6C	[7:0]	0x04	RW	aev	Dark edge clamp minus threshold value
dark_ec_pmax	D	70	[7:0]	0x7F	RW	aev	Dark edge clamp plus max value
dark_ec_mmax	D	74	[7:0]	0x7F	RW	aev	Dark edge clamp minus max value
dark_dc	D	7A	[7:0]	0x00	RW	aev	Dark de-color value
y_cont_th2	D	9A	[7:0]	0x80	RW	aev	Dark Y contrast th2 value
y_cont_slope2	D	9E	[7:0]	0x40	RW	aev	Dark Y contrast slope2 value

Table 62 Register Table - Group E

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
auto_control_1	E	04	[7:0]	0x98	RW	autov	Auto control
ext_inttime_h	E	22	[7:0]	0x00	RW	autov	Manual integration time @ external AE mode
ext_inttime_m	E	23	[7:0]	0x80	RW	autov	
ext_inttime_l	E	24	[7:0]	0x00	RW	autov	
ext_glbg_h	E	25	[7:0]	0x01	RW	autov	Manual analog gain @ external AE mode
ext_glbg_l	E	26	[7:0]	0x00	RW	autov	
exposure_t	E	27	[7:0]	0x00	RW	autov	Exposure
exposure_h	E	28	[7:0]	0x01	RW	autov	
exposure_m	E	29	[7:0]	0x40	RW	autov	
exposure_l	E	2A	[7:0]	0x00	RW	autov	

Table 63 Register Table - Group F

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pg_yt	F	08	[7:0]	0x7F	RW	aev	
pg_y1	F	09	[7:0]	0x73	RW	aev	
pg_y2	F	0A	[7:0]	0x02	RW	aev	
pg_y3	F	0B	[7:0]	0x08	RW	aev	
pg_y4	F	0C	[7:0]	0x0F	RW	aev	
pg_y5	F	0D	[7:0]	0x19	RW	aev	
pg_y6	F	0E	[7:0]	0x25	RW	aev	
pg_y7	F	0F	[7:0]	0x28	RW	aev	
pg_y8	F	10	[7:0]	0x38	RW	aev	
pg_y9	F	11	[7:0]	0x4E	RW	aev	
pg_y10	F	12	[7:0]	0x52	RW	aev	
pg_a	F	13	[7:0]	0xBF	RW	aev	
pg_b	F	14	[7:0]	0x81	RW	aev	
pg_c	F	15	[7:0]	0xBF	RW	aev	
pg_d	F	16	[7:0]	0x0B	RW	aev	Embedded parking guide line control
pg_e	F	17	[7:0]	0x0C	RW	aev	
pg_f	F	18	[7:0]	0x15	RW	aev	
pg_line1	F	19	[7:0]	0x21	RW	aev	
pg_line2	F	1A	[7:0]	0x23	RW	aev	
pg_line3	F	1B	[7:0]	0x24	RW	aev	
pg_line4	F	1C	[7:0]	0x46	RW	aev	
pg_line5	F	1D	[7:0]	0x48	RW	aev	
pg_line6	F	1E	[7:0]	0x42	RW	aev	
pg_line7	F	1F	[7:0]	0x4B	RW	aev	
pg_line8	F	20	[7:0]	0x71	RW	aev	
pg_line9	F	21	[7:0]	0x63	RW	aev	
pg_line10	F	22	[7:0]	0x74	RW	aev	
pg_center_h	F	23	[1:0]	0x01	RW	aev	
pg_center_l	F	24	[7:0]	0xE0	RW	aev	

Table 64 Register Table - Group G

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
str_ptr0_h	G	09	[7:0]	0xFF	RW		

Table 65 Register Table - Group H

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_blankEAV_f0	H	04	[7:0]	0xB6	RW		Blank EAV for field0 of CCIR656 data or blank EAV for frame data
sync_blankSAV_f0	H	05	[7:0]	0xAB	RW		Blank EAV for field1 of CCIR656 data or blank EAV for frame data
sync_activeEAV_f0	H	06	[7:0]	0x9D	RW		Active EAV for field0 of CCIR656 data or active EAV for frame data
sync_activeSAV_f0	H	07	[7:0]	0x80	RW		Active EAV for field1 of CCIR656 data or active EAV for frame data
sync_blankEAV_f1	H	08	[7:0]	0xF1	RW		blank EAV for field1 of CCIR656 data
sync_blankSAV_f1	H	09	[7:0]	0xEC	RW		blank SAV for field1 of CCIR656 data
sync_activeEAV_f1	H	0A	[7:0]	0xDA	RW		Active EAV for field1 of CCIR656 data
sync_activeSAV_f1	H	0B	[7:0]	0xC7	RW		Active SAV for field1 of CCIR656 data
sync_CCIR_FF	H	0C	[7:0]	0xFF	RW		CCIR data format
sync_CCIR_00	H	0D	[7:0]	0x00	RW		
sync_CCIR_80	H	0E	[7:0]	0x80	RW		
sync_CCIR_10	H	0F	[7:0]	0x10	RW		
enc_control1	H	9D	[7:0]	0x00	RW		Encoder control
setup_w	H	A9	[4:0]	0x07	RW		Setup time width
burst_duration	H	AB	[7:0]	0x00	RW		Burst duration
burst_slope_step	H	AC	[7:0]	0x38	RW		
sync_rising	H	AF	[3:0]	0x01	RW		horizontal rising time control of composite signal
enc_mode	H	B7	[1:0]	0xx	RW		Encoder mode
enc_sync	H	B8	[7:0]	0x10	RW		Encoder sync level
enc_blankH	H	B9	[7:0]	0x00	RW		Encoder blank level
enc_blankL	H	BA	[7:0]	0xx	RW		
enc_pedestal	H	BB	[7:0]	0xx	RW		Encoder pedestal
enc_burst	H	BC	[7:0]	0xx	RW		Burst amplitude
enc_Ygain	H	BD	[7:0]	0xx	RW		Y convergence gain from YCbCr to YUV
enc_Ugain	H	BE	[7:0]	0xx	RW		U convergence gain from YCbCr to YUV
enc_Vgain	H	BF	[7:0]	0xx	RW		V convergence gain from YCbCr to YUV
enc_Yrange_H	H	C0	[7:0]	0x03	RW		Max. luminance
enc_Yrange_L	H	C1	[7:0]	0x20	RW		
enc_Crange_H	H	C2	[7:0]	0x01	RW		Max. amplitudes of chrominance
enc_Crange_L	H	C3	[7:0]	0xx	RW		
enc_chroma_max_H	H	C4	[7:0]	0x03	RW		Maximum chrominance of composite output
enc_chroma_max_L	H	C5	[7:0]	0xx	RW		
enc_chroma_min_H	H	C6	[7:0]	0x00	RW		Minimum chrominance of composite output
enc_chroma_min_L	H	C7	[7:0]	0xx	RW		

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
enc_SCH_offset_T	H	E8	[7:0]	0x00	RW		SCH(subcarrier to horizontal) phase offset
enc_SCH_offset_H	H	E9	[7:0]	0x00	RW		
enc_SCH_offset_M	H	EA	[7:0]	0x00	RW		
enc_SCH_offset_L	H	EB	[7:0]	0x00	RW		
burst_toffset	H	ED	[7:0]	0x00	RW		Burst time +/- offset
encdat_rising	H	F2	[3:0]	0x01	RW		edge of the line blanking pulse rising time control
enc_scfreq	H	F3	[1:0]	0xx	RW		Subcarrier frequency selection for which TV mode

Table 66 Register Table - control register

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
i2c_control_1	A	23	[7:4]	4'b0101	RW		updatecontrol[3:0] control i2c register update by auto_vsync update_autov <= reg_updatecontrol(3) or (autov_update and reg_updatecontrol(2)) control i2c register update by ae_vsync update_aev <= reg_updatecontrol(1) or (aev_update and reg_updatecontrol(0))
clkdiv	A	25	[5]	1'b1	RW	aev	p_pp_equal pclk divider 0b : ppclk/2 1b : ppclk
	A	25	[2:0]	3'b000	RW	aev	ppclk_div[2:0] ppclk divider 000b : 1/1 001b : 2/3 010b : 1/2 011b : 1/3 100b : 1/4 101b : 1/8 else : 1/1
pad_control3	A	29	[7]	1'b0	RW		vsync_pad_en
	A	29	[4]	1'b0	RW		hsync_pad_en
	A	29	[3]	1'b0	RW		d1_pad_en
	A	29	[2]	1'b0	RW		d0_pad_en
	A	29	[0]	1'b0	RW		d_pad_selection
pad_control4	A	2A	[7]	1'b0	RW		ledctrl_en
pad_control6	A	2C	[7]	1'b0	RW		mirsctrl_en
	A	2C	[4]	1'b0	RW		irisctrl_en
pad_control8	A	2E	[7]	1'b0	RW		d9_pad_en
	A	2E	[6]	1'b0	RW		d8_pad_en
	A	2E	[5]	1'b0	RW		d7_pad_en
	A	2E	[4]	1'b0	RW		d6_pad_en
	A	2E	[3]	1'b0	RW		d5_pad_en
	A	2E	[2]	1'b0	RW		d4_pad_en
	A	2E	[1]	1'b0	RW		d3_pad_en
	A	2E	[0]	1'b0	RW		d2_pad_en
pad_control9	A	2F	[7]	1'b0	RW		d9_pad_manual
	A	2F	[6]	1'b0	RW		d8_pad_manual
	A	2F	[5]	1'b0	RW		d7_pad_manual
	A	2F	[4]	1'b0	RW		d6_pad_manual
	A	2F	[3]	1'b0	RW		d5_pad_manual
	A	2F	[2]	1'b0	RW		d4_pad_manual
	A	2F	[1]	1'b0	RW		d3_pad_manual
	A	2F	[0]	1'b0	RW		d2_pad_manual
pll_control1	A	4A	[5]	1'b1	RW		pll_pd PLL power down

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b0 : power on 1'b1 : power down
	A	4A	[4]	1'b1	RW		pll_bypass PLL bypass 1'b0 : use pll mode 1'b1 : pll bypass mode
flicker_control1	A	4F	[6]	1'b0	RW		fd_en flicker enable
	A	4F	[3]	1'b0	RW		manual_A
	A	4F	[2]	1'b0	RW		manual_B
led_control1	A	8E	[7]	1'b0	RW		ledctl en led control enable 0b : disable 1b : enable
	A	8E	[6]	1'b0	RW		ledctl manual led output value @ led control disable
	A	8E	[5]	1'b0	RW		ledctl polarity led output polarity change enable 0b : disable 1b : enable
	A	8E	[4]	1'b0	RW		bwled en black & white mode @ led on enable 0b : disable 1b : enable
	A	8E	[3]	1'b0	RW		mirs en moving IR/AR glass switch (MIRS) control enable 0b : disable 1b : enable
	A	8E	[2:1]	2'b00	RW		mirs manual mirs output value @ mirs control disable
	A	8E	[0]	1'b0	RW		mirs polarity mirs output polarity change enable 0b : disable 1b : enable
bayer_control_01	B	15	[6]	1'b0	RW		frmvar_en frame rate varying enable
	B	15	[1:0]	2'b01	RW		led_dsel[1:0] led data selection
bayer_control_02	B	16	[2]	1'b0	RW		inv_led led data inverting enable
isp_func_4	C	08	[7:6]	2'b00	RW	aev	win_show[1:0] ae window show enable 0b : disable 1b : enable
	C	08	[3]	1'b0	RW	aev	prvc_en privacy mode enable 0b : disable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1b : enable
format	C	29	[7:0]	8'b00001101	RW	aev	format_control[7:0] 0 : cbycry 32 : rrrr (for test only) 53 : rgb555 (byte swap) 1 : crycby 33 : gggg (for test only) 54 : rgb444 2 : ycbycr 34 : bbbb (for test only) 55 : rgb444 (byte swap) 3 : ycrycb 48 : rgb565 64 : raw bayer 16 : rggb 49 : rgb565 (byte swap) 65 : dpc bayter 17 : gbrg 50 : bgr565 66 : raw10 mipi (not used) 18 : grbg 51 : bgr565 (byte swap) 67 : mono 19 : bggr 52 : rgb555 68 : yyyy 128 : monitor
sync_control_0	C	9A	[6:5]	2'b00	RW	aev	sync_drop[1:0] 0 : disable 2 : vsync drop 1 : hsync drop 3 : hsync and vsync drop
sync_control_1	C	9B	[6]	1'b0	RW	aev	sync_vsyncPolarity vsync polarity change
	C	9B	[5]	1'b0	RW	aev	sync_hsyncAllLines hsync output all lines enable(black and active)
	C	9B	[4]	1'b0	RW	aev	sync_hsyncPolarity hsync polarity change
	C	9B	[3]	1'b0	RW	aev	sync_pclkwindow pclk window
	C	9B	[2]	1'b0	RW	aev	sync_pclkPolarity pclk polarity change
auto_control_1	E	04	[2]	1'b0	RW	au-tov	wb mode white blance mode selection 0b : auto mode 1b : manual mode
	E	04	[1:0]	2'b00	RW	au-tov	exposure mode[1:0] exposue mode selection 00b : auto mode 01b : manual mode (expsoure write) 10b : manual mode (ext_inttime, ext_glbgain write) 11b : manual mode (inttime, globalgain write)
auto_control_2	E	05	[3]	1'b0	RW	au-tov	fb gg globalgian selection @ front_black fitting 0b : high sensitivity conversion gain 1b : normal gain
enc_control1	H	9D	[3]	1'b0	RW		enc_chroma_kill TV encoder chroma signal kill enable@led ON(BW_mode) 0b : disable 1b : enable
	H	9D	[2]	1'b0	RW		burst kill TV encoder color burst kill enable@led ON(BW_mode) 0b : disable 1b : enable
	H	9D	[1]	1'b0	RW		manual_chroma_kill TV encoder chroma signal manual kill enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							0b : disable 1b : enable
	H	9D	[0]	1'b0	RW		manual_burst_kill TV encoder color burst manual kill enable 0b : disable 1b : enable

Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	24/08/2018	(Preliminary)	Sanghyun Han
0.1	12/09/2018	Add to key performance parameter	Sanghyun Han
0.2	21/09/2018	Edited Figure21	Yeari Seo
0.3	21/09/2018	Edit to X1 clock of PLL description	Sanghyun Han
0.4	26/02/2019	Modify to operation temperature	Sanghyun Han